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In My Opinion

Don't compromise on true Spice accuracy

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I talk to leading-edge analog and RF design teams every week -- literally hundreds of designers from over 100 companies in the last year alone. Their most common request is not a new analog methodology. What they want is a circuit simulator that produces true Spice accurate results much faster on much bigger circuits in both time and frequency domains.

Thus, I am surprised to see opinions like those expressed in two recent SCDsource.com articles, with industry experts promoting new methodologies and apparently dismissing Spice as behind the times (see: [Analog experts call for new methodologies](#), 02/08/08 and [Analog complexity demands new verification approaches](#), 12/19/07). Although new approaches may be valuable, they are no substitute for substantially better bread-and-butter circuit and RF simulation tools that deliver the accuracy, performance, and capacity required to verify today's complex blocks and full circuits. Such tools are here today, and design teams have proven them on hundreds of circuits on process nodes from 180 nm to 40 nm to deliver true Spice accuracy 5X-10X faster on 5X-10X larger circuits than traditional Spice simulators.

Analog/RF design teams are moving to 90 nm, 65 nm, 45 nm and below with multi-gigahertz frequencies, 1V power supplies, and CMOS processes. They are deeply concerned with issues such as post-layout verification, process variations that require extensive corner or Monte Carlo analysis, noise analysis on blocks such as sigma-delta ADCs and fractional-N PLLs, and verifying modulated data through full transmit and receive chains.

Those are just the basics. Don't forget full-circuit DC operating point analysis and full-circuit performance simulations. These are the only practical ways to know your circuit is connected correctly, the impact of electromigration on your circuit, and whether the circuit will perform to specifications in silicon.

All of the preceding verification tasks require true Spice accuracy, that is, waveforms identical to "golden" traditional Spice simulators down to the Spice noise floor or below. With significant effort, digital fast Spice simulators and behavioral approaches might get you to within 1% inaccuracy versus Spice. "Might" is an important word here, because you never know if you are 1% off or 5% off unless you actually run a true Spice accurate simulator.

That is just one fallacy of "accurate enough" simulation: it is impossible to know what is "accurate enough" unless you have a true Spice accurate result for comparison. The bigger problem is that digital fastSpice simulators are simply not accurate enough.

A 1% inaccuracy in analog/RF can easily mean the difference between successful silicon and a respin. To illustrate this point, we ran a true Spice accurate simulator on a production analog-to-digital

converter (ADC) with a relative tolerance (RelTol) of 1e-3 (Spice default), and then repeated the run with a RelTol of 1e-2 (a greatly relaxed tolerance) to approximate 0.1% inaccuracy and 1% inaccuracy respectively.

There was up to a 20 dB difference in signal-to-noise ratio (SNR) between the two runs. By comparison, the actual device noise increase on this circuit was only 10dB. Relying on a simulation with this level of inaccuracy for performance analysis, corner analysis, post-layout simulation, noise analysis, or periodic analysis is not just meaningless -- it is dangerous.

Consider the other extreme: inaccuracy in full-circuit simulations. As a simple example, consider a circuit that contains an ADC. With 1% inaccuracy, it is possible to verify only the most significant 6 bits of the ADC. That is hardly sufficient for today's ADCs, which are routinely 12 bits or larger. Although it may not be obvious, these simulators do not have the resolution necessary to verify the remaining six bit connections. The design team will not know about any lower-order bit disconnects or misconnects until the silicon fails to meet specifications. A true Spice accurate simulator would catch such problems during DC operating point analysis many weeks and hundreds of thousands of dollars sooner.

So, how do you know whether your circuit simulator is accurate? The simulator should find and maintain a true DC operating point, utilize the original device equations (making no device approximations), and solve the full original matrix at every timestep. Of course, the simulator should not require any netlist changes or tuning for individual blocks.

Next, test your simulator. Ensure that it produces waveforms that match your "golden" Spice simulator's results to the Spice noise floor. Better yet, where appropriate, post-process your results to get meaningful circuit metrics in the frequency domain, where minor differences that are difficult to see in waveforms will appear prominently. With the new generation of circuit simulators available on the market, there is no longer a need to compromise accuracy for performance or capacity.

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