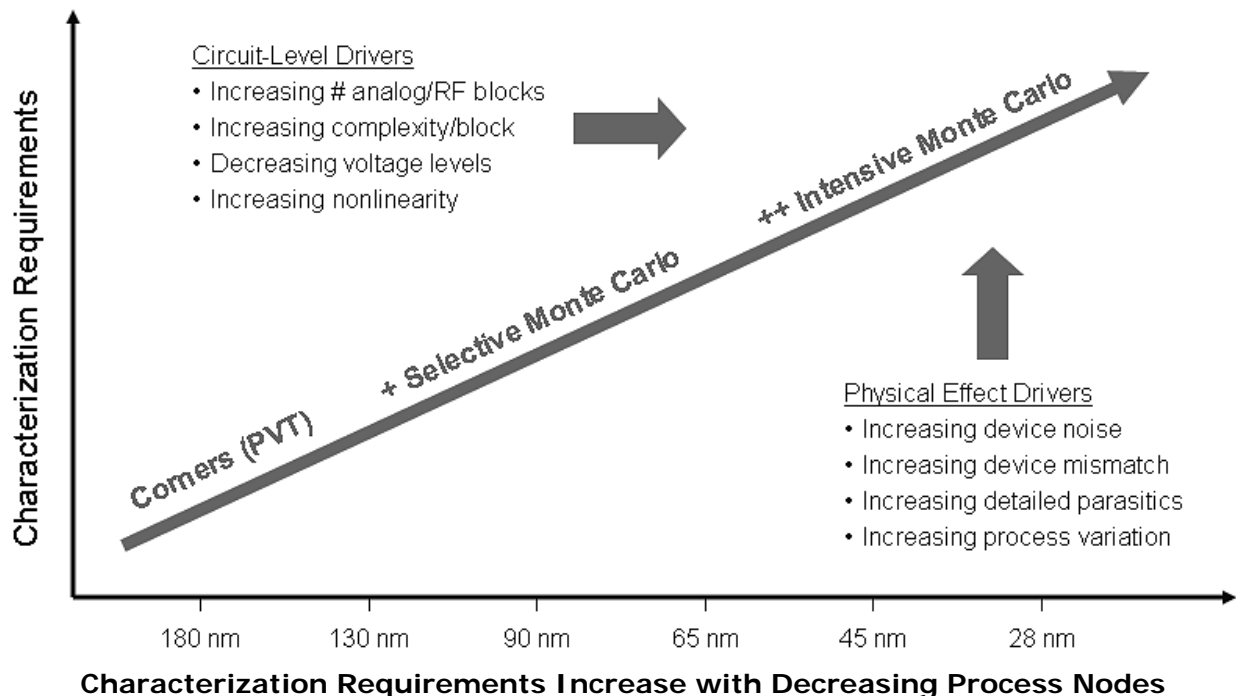


Analog FastSPICE Platform Application Brief Multi-Core Parallel for Analog/RF Block Characterization

The Problem

As analog and RF circuit designers move to lower process geometries, rigorous block characterization in the context of realistic physical effects becomes increasingly important. At 90nm and below, circuit complexity, circuit nonlinearity, and physical effects—including process variation, device noise, device mismatch, and detailed parasitics—make such characterization a growing computational bottleneck.



Traditional Block Characterization

Designers have traditionally run the desired corners, sweeps, and Monte Carlo iterations sequentially on a single machine with a single simulator. Given a practical total runtime limitation of at most a few days, this approach is increasingly inadequate. A distributed approach using scripts, an internal tool, or a third-party tool to distribute the iterations over a number of computers can reduce turnaround time or increase iterations in a given time. However, distributed characterization generally increase use model complexity, introduces turnaround time unpredictability, is subject to network issues, and requires a large number of simulator licenses.

AFS Platform for Traditional Block Characterization

The Analog FastSPICE unified verification platform (AFS) provides nanometer SPICE accuracy 5x-10x faster on a single core than traditional SPICE simulators. AFS also provides the industry's only silicon-accurate device noise analysis for every type of circuit. With batch mode and seamless integration into the industry's leading analog design environment, the AFS Platform plugs into current single-simulator or distributed characterization approaches without any changes, providing 5x-10x faster turnaround, 5x-10x more iterations, or any combination of the two.

AFS Platform: Multi-Core Parallel for Analog/RF Block Characterization

AFS Multi-Core Parallel (MCP) Block Characterization

The AFS Platform provides a multi-core parallel operating mode that dramatically speeds analog/RF block characterization on shared-memory multi-core systems. AFS MCP automatically runs corner, sweep, or Monte Carlo iterations in parallel on separate cores—each of which runs 5x-10x faster than traditional SPICE. With limited overhead the net speedup versus traditional SPICE on a single-core machine is ~15x-30x on 4 cores and ~30x-60x on 8 cores. This speedup is reduced in cases with significant runtime variance per iteration (e.g., with some RF analysis sweeps). MCP supports all AFS Platform analyses. Running it requires simply specifying the desired number cores—the rest of the inputs and all of the outputs are the same as single-core operation.

AFS MCP Characterization Speedup Examples for Analog and RF Circuits

Circuits				Speedup versus 1-core AFS		
Circuit	Analysis	Elements	MOS	2 Core	4 Core	8 Core
VCO	transient	1.5K	1.2K	2.0x	3.3x	5.0x
ADC	transient	17K	15.4K	1.9x	3.6x	5.7x
DLL	transient	127K	4.3K	N/A	3.9x	7.8x
Transmitter	transient	750K	15.2K	1.9x	3.7x	7.0x
Mixer	RF	26	3	1.9x	2.8x	4.5x
Ring VCO	RF	101	80	1.9x	3.8x	5.2x
LNA IP3	RF	174	8	1.7x	2.2x	4.0x
DSM IP3	RF	1.4K	135	1.8x	3.5x	4.5x

AFS MCP Cost and Licensing Advantages

Analog FastSPICE multi-core parallel licensing is very compelling. AFS MCP requires only one additional BDA Token to run on up to 4 cores and only two additional BDA Tokens to run up to 8 cores. Thus, 3 BDA Tokens can perform the same characterization run on a single machine as would require literally 24 to 50 traditional SPICE or “parallel” SPICE licenses on 6 to 50 machines. This advantage applies to any type of iterative run with any type of analysis (e.g., transient Monte Carlo and RF sweeps).

Analog FastSPICE Platform Analyses Support

- AFS circuit simulation: .dc, .ac., noise, transient
- Monte Carlo (including Latin Hypercube Sampling), sweeps, alter/altergroup
- AFS transient noise analysis
- AFS RF: periodic steady state, periodic noise, PAC, PXF, harmonic balance
- AFS Co-simulation

Environment Support

- Batch/command line
- Cadence OCEAN V5.1 and V6.1
- Cadence Virtuous Analog Design Environment V5.1 (V6.1 planned)