Big Analog/RF Verification:

Complex-Block Characterization
&
Full-Circuit Performance Simulation

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1 Introduction

Today's analog/RF verification methodologies are severely tool limited. Characterizing complex blocks and running full-circuit performance simulation is impossible using traditional SPICE and digital fastSPICE tools. Circuit designers work around today's simulator accuracy, performance, and capacity limitations to verify as much as possible and then hope their silicon is functional and meets spec. In the face of increasing circuit complexity, new physical effects, complex device models, low voltages, GHz frequencies, nanometer bulk processes, tighter specs, and short market windows, this approach has hit a wall.

Berkeley Design Automation is tearing down that wall with its Precision Circuit Analysis™ technology. The first major breakthrough in analog and RF verification technology in decades, the technology delivers:

- Identical waveforms as traditional SPICE down to the SPICE noise floor
- 5x-10x higher performance
- 5x-10x higher effective capacity
- No block-level tuning (i.e., no need to tradeoff accuracy for speed)
- No netlist, model, environment, or flow changes

The real breakthrough lies in not compromising at all on true SPICE accuracy while delivering vastly superior performance and capacity. Initially skeptical, design teams from >50 companies have validated these claims on hundreds of production circuits. Many of these teams are now using Berkeley Design Automation technology to solve big analog/RF verifications problems that were previously impossible or impractical, specifically:

- Complex-block characterization: pre-layout simulation, post-layout simulation, variation analysis, noise analysis, and periodic analysis of complex blocks such as PLLs, sigma-delta ADCs, transmit chains, receive chains, DC:DC converters, and memories.
- Full-circuit performance simulation: DC operating point analysis, functional verification, package and transmission-line analysis, and targeted performance simulation of full circuits including 802.11 transceivers, WCDMA transceivers, microcontrollers, power converters, data converters, and digital TV tuners, and wireline transceivers.

Through extensive real-world examples this paper presents the state-of-the-art in big analog/RF verification as enabled by Berkeley Design Automation technology. It is based on working closely with numerous design teams from top-tier semiconductor suppliers to world-class startups on production circuits often under tremendous tapeout pressure. In all cases the circuits are real, the accuracy is designer-verified to the SPICE noise floor, and performance comparisons are based on using equivalent compute hardware.

2 Traditional SPICE, Digital FastSPICE, and Analog FastSPICE

EDA companies are notorious for making exaggerated and misleading claims. In the circuit simulation area, EDA companies have and continue to make claims of “full SPICE accuracy” for simulators that cannot produce identical waveforms as SPICE and “5x-10x performance” when this is possible under only very limited conditions. As a result, design teams are understandably skeptical about circuit simulation accuracy and performance claims. Unlike other companies, Berkeley Design Automation (BDA) bases its claims solely on empirical results, sets conservative expectations, and ensures it delivers to those expectations.

Berkeley Design Automation Analog FastSPICE™ Platform (AFS Platform) is a unified circuit verification platform that provides analog, mixed-signal, and RF (AMS/RF) design teams the ultimate in accuracy, performance, capacity, and functionality. The AFS Platform delivers true SPICE accuracy, 5x-20x higher performance, >10M-element capacity, and advanced analyses. Based on extensive experience benchmarking against all leading transistor-level simulators, BDA can confidently classify all of them into one of two categories: traditional SPICE or digital fastSPICE. Traditional SPICE simulators maintain true SPICE accuracy with limited performance and capacity. Digital fastSPICE simulators compromise some accuracy (dependent on block-based simulator tuning) for higher performance and capacity.

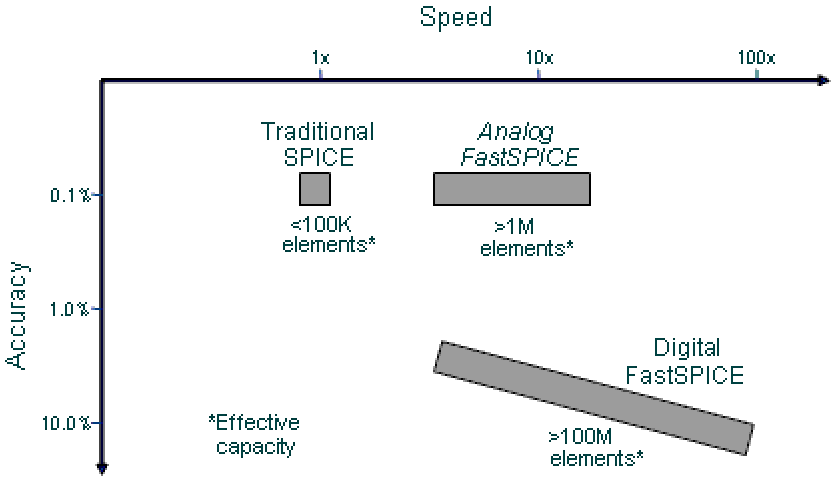

Figure 1. Circuit Simulator Category Comparison

<u>Traditional SPICE</u>

Traditional SPICE tools use the following techniques to ensure “true SPICE accuracy”:

- Create a flat netlist
- Find and maintain a true DC operating point
- Utilize global tolerance settings only (most notably reltol)
- Utilize the original device equations (make no device approximations)
- Solve the full original matrix at each iteration of each time-step

The IC community universally grants the two market leading SPICE simulators “golden” accuracy status. These simulators’ waveforms are the reference for all Berkeley Design Automation accuracy comparisons.

Traditional SPICE tools work well for simple blocks, e.g., those with <10K elements and <1 hour transient runtimes. However their performance and capacity are inadequate for thoroughly characterizing complex blocks and they fail to converge for many top-level analog/RF circuits.

Digital FastSPICE

Digital fastSPICE tools are circuit simulators that sacrifice some accuracy in order to provide increased performance and/or capacity relative to traditional SPICE. Some of the techniques they use that sacrifice accuracy are:

- Do not generate or maintain a DC operating point
- Utilize simplified device models
- Partition into sub-circuits and independently solving the matrix for each
- Use event-driven simulation
- Require block-level simulator tuning
- Utilize hierarchy to represent “redundant” circuitry

Despite marketing claims to the contrary, it is simply not possible to use any of the above techniques without compromising some degree of accuracy (which is why traditional SPICE simulators do not use these techniques even though they have been available for over a decade).

The name “digital fastSPICE” is intended to make it clear that these simulators are well suited for digital designs (e.g., memories and SoCs) that require potentially orders of magnitude more performance and/or capacity than traditional SPICE and for which up to 10% (or potentially more) inaccuracy is sufficient. Digital fastSPICE simulators are a fundamental mismatch for analog and RF circuits, because virtually any inaccuracy in the simulation of analog/RF circuits can lead to a qualitatively (i.e., functionally) different result; this is totally unacceptable when designers require results that are quantitatively accurate to the millivolt or milliamp range (~0.1%).

Many analog/RF design teams use or have used digital fastSPICE for “functional verification” (i.e., to check qualitative behavior) on analog/RF circuits. Doing so requires sometimes extensive block-based simulator tuning. The tuning methodology requires designers to select an initial set of simulator accuracy parameters for each block, run a simulation, check the results, adjust the simulation parameters (tightening blocks that seem to have incorrect or insufficient behavior and loosening blocks where accuracy seems “good enough” but performance is low), and repeat until the overall behavior looks “good enough” and the simulation is fast enough (or the designer gives up). Beyond the obvious problems of lost designer productivity, lost time, and considerable resource underutilization (tool and hardware), the core problem is that there is no reference for determining whether any results really are “good enough.” Many analog/RF designer teams will not even try digital fastSPICE for these reasons. As one design manager put it, “digital fastSPICE simulators are the fastest way to get the wrong answer.”

Multi-mode SPICE/Digital FastSPICE Tools

Several EDA companies now offer multi-mode simulators that include traditional SPICE and digital fastSPICE modes. The marketing messages make it seem like these simulators produce true SPICE accurate results with much higher performance and capacity than traditional SPICE. The fact is that these simulators are in fact separate traditional SPICE and digital fastSPICE engines, and users can have the results associated with one or the other type of simulator – not the best of both worlds. If these simulators could simultaneously deliver the best of both worlds, they would not need multiple operating modes.

Analog FastSPICE

Berkeley Design Automation Analog FastSPICE Platform (AFS Platform) includes the AFS Circuit Simulator (AFS), the only known simulator to produce true SPICE accuracy with 5x-20x higher performance and >10M-element capacity. This paper uses the label “true SPICE accuracy” to mean identical waveforms to traditional SPICE down to the SPICE noise floor. The AFS Platform 5x-20x performance and effective capacity advantages are compared to any simulator that also produces true SPICE accuracy. The AFS Platform also includes AFS RF, periodic analysis capability, with similar accuracy, performance, and capacity characteristics.

The company has established the foundation for its accuracy, performance, and capacity claims based on benchmarks with literally hundreds of production circuits. These claims are not hype, and there is no magic behind them – only solid, innovative engineering. BDA uses the traditional SPICE techniques stated above to ensure it always delivers true SPICE accuracy (i.e., it creates a flat netlist, finds and maintains a true DC operating point, utilizes global tolerance settings only, utilizes the original device equations without approximations, and solve the original matrix at every time step). Contrary to other simulator companies, rather than compromise accuracy BDA is pushing accuracy to a new level and often provides provably better accuracy than traditional SPICE. This increased accuracy is needed to accurately deliver analysis beyond transient simulation, e.g. noise analysis and periodic analysis.

The tool’s exceptional performance and capacity are not the result of a single “silver bullet,” but of many “silver bullets.” BDA started with a new clean, modular simulator architecture that enables the company to independently optimize every major area within the simulator. BDA systematically applies the latest numerical analysis techniques to optimize each area without compromising accuracy. Enough silver bullets hit every circuit to deliver at least 5x performance; however, many more silver bullets hit some circuits resulting in 10x, 20x, or sometimes even greater performance benefit. Even with its significant lead, BDA sees considerable room for additional performance advances.

3 Evaluation Methodology: Accuracy, Performance, Capacity, and Compatibility

Terms like accuracy, performance, capacity, and compatibility are overloaded and often abused. This section defines specifically how Berkeley Design Automation uses these terms to establish a common engineering baseline for simulator comparisons.

<u>Accuracy Comparisons</u>
All AFS Platform accuracy comparisons are relative to the two industry leading "golden" simulators. BDA guarantees identical accuracy to the SPICE noise floor when compared to these simulators' results. That standard is built into the technology in that the AFS Platform solves the original device equations, the full circuit matrix, and takes no algorithmic shortcuts that could compromise accuracy. The simulator noise floor is the effective resolution based on a number of global SPICE settings most notably reltol, time-step control, and signal amplitude. Generally it is within ~0.1% of the magnitude of the desired signal.

All accuracy comparisons are based on running the same netlist and models in both simulators. AFS respects the same accuracy settings as the leading simulators (e.g., reltol, abstol, gmin, minstep, and maxstep). All comparisons start with both traditional SPICE and AFS using the same moderate or high (preferred) accuracy settings. BDA sets its defaults more conservatively than the leading traditional SPICE simulators, so if there is a difference AFS is generally more accurate. Given subtle simulator algorithm differences in rare cases it is necessary to make minor adjustments to these settings to get equivalent results.

The designer – not BDA – is always the standard for assessing accuracy. Designers typically compare accuracy using waveforms comparisons (e.g., overlays and measurements at specific nodes) or post processing (i.e., computations based on waveforms or measurements, e.g. to determine PLL jitter, power spectral density, etc.). In cases where these are not practical (e.g., traditional SPICE cannot produce results), designers often use one or more of the following: comparison to silicon, other simulation methods (e.g., AMS or system-level numerical analysis), and engineering analysis.

Since AFS is inherently SPICE accurate, BDA encourages designers to report any SPICE accuracy discrepancies above the simulator noise floor. The first step in debugging any discrepancy is to tighten the tolerances in both simulators. More often than not the traditional SPICE waveforms move toward the AFS waveforms which remain relatively stable through the tolerance-tightening process. This indicates that the AFS waveforms were indeed more accurate. As designers tighten tolerances for traditional SPICE, runtimes increase significantly and often it begins to fail to converge. This scenario is common, and designers are literally awestruck when it occurs. Of course AFS is not perfect. If a discrepancy remains even with very tight tolerances, BDA isolates the cause and fixes any associated bug.

Performance Comparisons

All AFS Platform performance comparisons are versus other simulators that have also produced true SPICE accurate results. The AFS Platform achieves its performance advantage through computational efficiency that is fully effective for circuits with at least moderate complexity. AFS consistently delivers at least 5x performance versus traditional SPICE for circuits that are at least 1K elements and have >1-hour runtimes. BDA does not focus on smaller circuits because traditional SPICE performance and capacity is sufficient for them. Despite their size, circuits with very high parasitic-to-transistor ratios can also be computationally simple. AFS consistently delivers at least 5x higher performance versus traditional SPICE for circuits where the ratio is 10 or less.

AFS comparisons use the same netlist with the same or equivalent accuracy settings as traditional SPICE. After running the netlist as is, BDA removes any settings that the designer may have made to help the traditional SPICE simulator with convergence, accuracy, and performance (e.g., gmin, DC convergence method settings, abstol, reltol, and time-step control). AFS generally does not need this “help” and can produce accurate results within the SPICE noise floor with even higher performance without it.

All AFS performance comparisons are also based on equivalent hardware and operating system.

Capacity Comparisons

Berkeley Design Automation makes a distinction between load capacity and effective capacity – a distinction that is important for any simulator. Load capacity is a simulator’s required memory footprint for a given netlist. AFS creates a flat netlist like traditional SPICE. Its memory footprint is comparable and generally somewhat smaller than traditional SPICE.

Effective capacity is a simulator’s true useful capacity. It is a function of achieving DC convergence and performance. AFS has far superior DC convergence to traditional SPICE tools. Traditional SPICE tools can generally converge on netlists up to 100K elements or so, although there are many cases where they fail on substantially smaller circuits (e.g., those with complex device models). AFS routinely converges on circuits with >1M total elements and >250K transistors and has often gone much higher (e.g., >2M total elements and >1M transistors). Just as importantly, its superior performance enables AFS to complete large true SPICE accurate simulations in a timeframe of relevance.

AFS does not use hierarchical partitioning. It is not intended to handle complete SoCs or large memories with tens-of-millions of elements such as those that digital fastSPICE tools can handle. BDA uses the term “full-circuit” to refer to a top-level analog/RF circuit with perhaps limited transistor-level digital logic (such that it fits within the AFS effective capacity) – not a transistor-level representation of a primarily digital design (e.g., an entire SoC or full memory IC).

Compatibility

The AFS Platform has true "plug-and-play" capability in the leading analog/RF circuit design flows. It utilizes standard Synopsys® HSPICE® circuit simulator and Cadence® Virtuoso® Spectre Circuit Simulator netlists without modification. Netlist compatibility is particularly challenging because there are an astronomical number of corner cases including those due to undocumented, ambiguously documented, and incorrectly documented "features." Whenever practical, BDA begins an evaluation by bringing a small number of circuit testcases in house to address any incompatibility issues. In most cases this process takes only a few days. Running through a few circuits for any given design group generally cleans up any and all compatibility issues for that group.

The AFS Platform supports standard HSPICE and Spectre models without modification including BSIM 3, BSIM4, JFET, Gummel Poon, HICUM, VBIC, Mextram, BSIMSOI, Verilog A, b-sources, w-elements, s-parameters, and others. The AFS Platform is fully integrated into the Cadence® Virtuoso® Analog Design Environment (a.k.a., "Analog Artist") in which it is accessible via a pull-down menu option, uses the same forms, back-annotates to the schematic, etc. It also produces a number of common output formats including PSF (binary and ASCII) and tr0 for use with standard waveform tools.

4 Big Analog/RF Verification: Complex-Block Characterization

Designers tackle two distinct categories of Big Analog/RF Verification problems: complex-block characterization and full-circuit performance simulation. This section focuses on the former and the next section on the latter.

For the purposes of Big Analog/RF Verification, a "complex block" is defined as meeting the following two requirements:

- The block has critical emergent functional and performance characteristics that cannot be accurately analyzed through decomposition.
- Traditional SPICE cannot complete the desired analysis in a timeframe of relevance due to speed limitations or at all due to DC convergence limitations.

Common complex blocks in today's designs include ADCs (sigma-delta and pipelined), PLLs (fractional-N and integer-N), DLLs, DC:DC converters, PHYs, CDRs, frequency synthesizers, transmit chains, and receive chains.

Complex blocks are often very sensitive and highly nonlinear. Even minor simulation inaccuracies can lead to results that are not just quantitatively incorrect, but actually qualitatively incorrect, i.e., functionally wrong. In fact, it is often desirable and sometimes even necessary to run complex blocks with tighter than the default SPICE tolerances in order to push down the noise floor for even pre-layout simulations. Of course designers avoid this whenever possible because it slows down simulation and can even lead to problems getting or maintaining DC convergence.

Since complex blocks have performance-critical emergent properties, it is highly desirable to characterize them as a whole just as thoroughly as one would characterize performance-critical simple blocks. Characterization includes some or all of the following:

1. Pre-layout transient simulation
2. Post-layout transient simulation
3. Variation analysis (corners analysis or Monte Carlo)
4. Noise analysis
5. Periodic analysis (RF circuits)

Pre-layout Transient Simulation

Of these techniques, pre-layout transient simulation is by far the simplest, least time consuming, and least demanding in terms of simulator accuracy (i.e., a low noise floor). Yet designers are struggling to complete enough pre-layout transient simulation for complex blocks with their current tools.

Consider phase-locked loops, for example. PLLs have notoriously long transient runtimes, in part due to the widely disparate frequencies which can range many orders-of-magnitude (e.g., kHz to GHz). Designers need to verify that PLLs lock correctly and check key metrics such as control voltage, charge-pump current, frequency, and output jitter. Pre-layout transient runtimes for high-frequency, nanometer PLLs generally range from multiple days to over a week using traditional SPICE.

PLLs' characteristics make them a favorite for designers to try using digital fastSPICE. The reasoning is: 1) digital fastSPICE can take advantage of PLL sub-circuits' widely different frequencies through block-level tuning to reduce simulation time, and 2) digital fastSPICE provides "good enough" accuracy because locking simulations are primarily functional. Designers know that using digital fastSPICE requires hours or even days of tuning and they know that not having true SPICE accuracy introduces risk, but many figure that these downsides are worthwhile when the only option is extremely long traditional SPICE runs that introduce known schedule risk.

Perhaps because PLLs have been a favorite analog application for digital fastSPICE, they are also a common example of failed silicon. The first time a PLL designer sees functionally inaccurate behavior from a digital fastSPICE simulator (i.e., a PLL seems to lock when the circuit actually won't lock or vice versa), they generally never again believe digital fastSPICE accuracy is "good enough." Lucky design teams catch these problems by checking a suspicious result with traditional SPICE. The unfortunate ones see the real PLL behavior for the first time in silicon.

Sigma-delta ADCs, which also contain frequencies that can range orders-of-magnitude, are an example of circuits at the other extreme from PLLs in that they often require accuracy that is tighter than the traditional SPICE defaults deliver. Designers must tighten tolerances and time-steps, which considerably slows traditional SPICE and sometimes causes it to stop converging. Digital fastSPICE tools have no place here.

Other complex blocks have transient accuracy requirements somewhere between PLLs and sigma-delta ADCs. Most have runtimes that are many hours to many days long. Even those at the shorter end of this spectrum can be problematic when they require many iterations; 4-hour runtimes mean designers get only 3 iterations per day (one based on overnight runs and 2 based on daytime runs).

Table 1. Complex-Block Pre-Layout Transient Examples

Circuit	Elements	MOS	SPICE	BDA	Speedup
PLL (3GHz, 130nm)	6K	4K	21 days	20 hrs	22x
PLL (3GHz)	4K	3.8K	78 hrs	5.4 hrs	14x
Sigma-Delta ADC	6K	5K	105 hrs	14 hrs	7x
Pipeline ADC	4K	3.8K	18 hrs	3.2 hrs	6x
Video ADC	5.8K	5.6K	7 hrs	25 min	15x
Multi-channel DC:DC	12.5K	8.4K	DNC[1]	3.1 days	Infinite
Power IC DC Converter	38.6K	33.4K	6.5 days	18 hrs	8.6x
Rx Chain	40K	38K	19 hrs	4 hrs	5x
Frequency Synthesizer	10.5K	5K	8.5 days	20 hrs	9x
AGC w/bandgap & bias	16K	–	13 hrs	22 min	36x

Notes:
1. Did not converge.

Table 1 shows a number of examples with traditional SPICE runtimes versus Berkeley Design Automation AFS circuit simulation runtimes. Unless otherwise noted, throughout this paper all comparisons are with one of the industry's two leading "golden" SPICE simulators. All examples utilize the original netlist and the designer verified the AFS waveforms matched traditional SPICE down to the SPICE noise floor (generally 0.1% or tighter with reltol = 1E-4 or less). All performance numbers are based on equivalent hardware.

Berkeley Design Automation consistently delivers at least 5x higher performance with identical or better accuracy for circuits with >1K elements and >1 hr runtimes. The impact of doing so on these circuits is dramatic. In the first PLL example, AFS turned 3 weeks into less than 1 day, and by doing so turned an impractical verification task into one that is quite manageable. This is admittedly a rather extreme example. The next example is a more typical PLL where AFS delivered 14x, slashing over 3 days to less than 5.5 hours. The next three examples are ADCs. AFS took the 4-day sigma-delta ADC run from over 4 days to about a 1/2 day, the pipelined ADC from overnight to 3.2 hours, and the video ADC from 7 hours to 25 minutes.

DC converters are another class of circuits that require long transient simulations with true SPICE accuracy. Even though it is only 12.5K total elements, the multi-channel DC:DC did not converge in traditional SPICE. AFS converged and finished the required transient simulation in a little over 3 days. The power IC DC converter is much larger with 33.4K transistors. Traditional SPICE did converge on this circuit, but it took nearly 1 week to simulate what AFS completed in less than 1 day – with identical accuracy.

The remaining circuits are a receive chain, frequency synthesizer, and automatic gain control circuit with bandgap and bias. AFS completed these pre-layout simulations 5x, 9x, and 36x faster, respectively, than the design teams' traditional SPICE simulator. It bears repeating that in all cases in this paper, AFS delivered these performance numbers while delivering waveforms that the designer verified were at least as accurate as their "golden" traditional SPICE simulator.

As would be expected, designers for most these circuits were skeptical prior to running AFS. After running the tool themselves and verifying the accuracy of the results, many were literally astonished. They firmly believed that the only way to get higher performance was to compromise accuracy. They believed that BDA was exaggerating either its claims or not fully disclosing some tool limitation. Once designers experience BDA accuracy and performance firsthand, they immediately try it on even more challenging problems. With complex blocks, that means more detailed characterization, generally starting with post-layout transient simulation.

Post-layout Transient Simulation

In today's complex blocks, designers disregard parasitics at their risk. During pre-layout verification designers include the most critical parasitics only, i.e., those they expect to have first-order functional and performance effects. Designers run post-layout transient simulation to see second-order performance effects, as well as to verify their choices for critical first-order parasitics in the pre-layout simulation.

Post-layout netlists generally have on the order of 4x-10x more total elements than the equivalent pre-layout netlist, although the number can sometimes be much higher. Resistors and capacitors dominate the total count, but parasitics increasingly include inductance and even mutual inductance. Even though Rs and Cs are simple components, the total element count often increases beyond 100K elements. In many cases traditional SPICE simulators simply cannot converge on such circuits. When traditional SPICE does converge, the runtimes can be 2x-4x or longer versus the circuit's pre-layout simulation. Digital fastSPICE simulators generally do not even have sufficient accuracy for pre-layout simulation. Even designers who use digital fastSPICE for pre-layout generally consider applying them post layout is a waste of time because their results will be misleading at best. This is often a moot point because of digital fastSPICE's notoriously poor support of inductors.

Table 2. Complex-Block Post-Layout Transient Examples

Circuit	**Elements**	**MOS**	**SPICE**	**BDA**	**Speedup**
Sigma-Delta ADC (3rd)	69K	5K	DNC[1]	29 hrs	Infinite
DLL	203K	18.3K	1.8 days	7.3 hrs	6x
PLL (1.6GHz, 65nm)	43K	2.9K	3.4 wks	3.2 days	7x
Sigma-Delta ADC (3rd)	64K	15K	5 days	4.5 hrs	25x
Video ADC	842K	11.3K	8.6 days	16 hrs	13x
Bias Circuit	100K	1K	DNC[1]	48 min	Infinite
VCO (RLCK)	186K	342	22 hrs	1 hr	22x

Notes:

1. Did not converge.

The first circuit in Table 2 exemplifies the problems with SPICE and digital fastSPICE for post-layout complex blocks. It is a 3rd-order sigma-delta ADC with ~14x more parasitics than transistors. SPICE did not converge (DNC), so the designer tried digital fastSPICE. After block-level tuning the designer got digital fastSPICE to complete a run in 333 hours – that's about 1.5 weeks and 18x longer than the pre-layout SPICE run. Fortunately in this case the designer was evaluating the simulator on a circuit that was already in silicon. The digital fastSPICE SNR was off by 5 dB. Not surprisingly the designer deemed the accuracy unacceptable and decided not to use digital fastSPICE for such applications in the future. The designer tried AFS on the exact same netlist and was astounded that the tool completed transient in just 29 hours with results within 1 dB of silicon.

The other examples also clearly demonstrate how AFS easily handles otherwise impractical or impossible problems. The DLL has over 200K total elements; AFS reduced the runtime from 1.8 days to 7.3 hours. Few design teams have 3.4 weeks to run the post-layout PLL, but most would be willing to spend the 3.2 day AFS runtime to check it. The next example is a second sigma-delta ADC in which AFS was 25x faster.

The last three circuits have especially high parasitic-to-transistor ratios. The video ADC is the post-layout version of the pre-layout video ADC in Table 1. There were 842K total elements and 11.3K transistors in the post-layout netlist for a ~75x ratio. Traditional SPICE was able to converge and complete transient analysis in 8.6 days. AFS took only 16 hours. This 13x speedup is comparable to the 15x speedup pre-layout. The bias circuit had a 100x ratio, did not converge in SPICE, and finished in just 48 minutes using AFS. The last circuit, a VCO, included inductors and mutual inductors in addition to resistors and capacitors and had an overall parasitic-to-transistor ratio over 45x. The designer's "golden" SPICE simulator took 22x longer than AFS to produce the same results.

Variation Analysis

Nanometer-scale analog/RF circuits are very susceptible to variations in process, voltages, and temperatures, especially when implemented in CMOS. Given the level of integration and associated mask set and silicon costs, ensuring yield prior to tapeout is increasingly important. Doing so requires running across an increasing number of corners or moving to Monte Carlo. Generally this means running 10, 100, or more full accuracy transient simulations – potentially including parasitics. These simulations absolutely require true SPICE accuracy to trust the quantitative results, let alone discern the sometimes subtle variances between iterations. This massive task occurs at the end of the design cycle where schedule pressures are highest and compute resources are often at a premium.

Table 3. Complex-Block Variation Analysis Examples

Circuit	Elements	MOS	SPICE	BDA	Speedup
PLL (65nm), 50-60 corners	13.6K	7.3K	7-10 days	20 hrs	9x
PLL (6/12 GHz), 7 corners	4.7K	1.1K	2.3 days	2.6 hrs	20x
Burst Read Path, 9 corners	97.4K	45.6K	2.5 days[1]	2 hrs	30x
Amplifier, Monte Carlo	1.1K	712	4.6 hrs	33 min	8.5x

Notes:
1. Required digital fastSPICE to compute initial conditions for SPICE run.

The first example in Table 3 is a 65nm PLL for a high-volume, high-end SoC. The design team used extensive corner analysis to ensure the circuit was going to have sufficiently high yield. Their traditional SPICE simulator took 7-10 days to run each corner. In order to get this done as quickly as possible, they set up a dedicated 30-server farm running traditional SPICE. Even so, it took >2 weeks to complete. Just as importantly, since each run took at least a week they could not get their first results back until that long. One AFS license running on a single-CPU finished a corner in 20 hours – 9x faster with identical results for every node. With only 5 AFS licenses, the design team could finish the analysis in about half the time as their 30-SPICE simulator farm – and they would get results from the first 5 corners in less than 1 day, the next 5 in less than 2 days, etc. So, they could catch any early problems up to 6 days sooner. When the design team subsequently ran a new 55nm PLL, traditional SPICE took 3-4 weeks to complete a corner. AFS completes a corner in 3-4 days.

The second PLL in Table 3 was also targeted for a high-volume SoC. Although the designers wanted to run Monte Carlo with at least 50 iterations, they deemed doing so as infeasible because each iteration required 2.3 days with their traditional SPICE simulator. AFS delivered the identical results in only 2.6 hours – 20x faster – making Monte Carlo practical.

The Burst Read Path example is one of many tests for a leading-edge flash memory circuit. Traditional SPICE could not converge on the circuit, which had nearly 100K total elements and over 45K transistors. To get around this problem, the designer ran a digital fastSPICE simulator to generate initial conditions to feed into their traditional SPICE simulator. The same setup worked for 4 corners at most, so the designer needed to change the setup several times to complete all 9 corners. The total runtime was 2.5 days per corner. AFS converged and ran every corner with no need for fastSPICE-generated initial conditions and each corner required only 2 hours – 30x faster.

The final example in Table 3 illustrates the value of AFS for modest-sized circuits that require extensive Monte Carlo analysis. The designer was running a 500-iteration Monte Carlo analysis on an amplifier that had only 1.1K total elements. The total runtime was 4.6 hours, which is ~33 seconds per iteration. Although Berkeley Design Automation targets much larger simulations with AFS, in this case the tool delivered identical results 8.5x faster, cutting each iteration to less than 4 seconds.

Noise Analysis

Noise has a dramatic effect on system-level performance, e.g., signal-to-noise ratio (SNR) and bit-error rate (BER). Designers of low-voltage, high-frequency circuits ignore noise at their own risk. That risk goes up significantly with circuits that have noise sensitive architectures, tight specifications, and are implemented on bulk CMOS processes. Most common complex blocks are highly susceptible to noise, including sigma-delta ADCs, fractional-N PLLs, integer-N PLLs, and high-speed I/Os.

Noise analysis should include random (thermal and flicker) and deterministic noise sources. There are three primary transistor-level noise analysis techniques:.

- Transient Noise Analysis: injects noise for each node at each time-step during transient simulation to produce output waveforms that include the effects of realistic noise. Designers post-process the noisy waveforms to determine the noise effect. This technique is valid for all types of circuits and is the only transistor-level noise analysis technique for non-periodic circuits such as sigma-delta ADCs and frac-N PLLs. Some traditional SPICE simulators offer transient noise analysis; however it is so notoriously slow that it is infeasible in most cases.

- Periodic Noise Analysis (pnoise): directly analyzes noise in periodic driven circuits such as dividers, switch cap filters, and phase detectors. Pnoise analysis is faster than transient noise analysis for this type of circuit and provides additional diagnostic information (e.g., individual noise source contributions). Traditional RF simulators (Shooting-Newton and harmonic balance) have periodic-steady-state convergence problems for complex periodic circuits and inherently tradeoff accuracy, performance, and capacity.

- Oscillator Noise Analysis (oscnoise/vconoise): directly analyzes noise in periodic autonomous circuits such as VCOs (LC-tank and ring oscillator) and crystal oscillators. Oscnoise/vconoise analysis is faster than transient noise analysis for this type of circuit and provides additional diagnostic information (e.g., individual noise source contributions). Traditional RF simulators have periodic-steady-state convergence problems for complex periodic circuits; make inherent approximations that adversely effect accuracy; and inherently tradeoff accuracy, performance, and capacity.

A simple methodology analyzing noise in complex blocks starts with the component sub-circuits. The first step is to apply periodic noise and oscillator noise to sub-circuits within a complex block wherever applicable because these techniques are faster and provide superior diagnostics to transient noise. In parallel, apply transient noise to all other sub-circuits. Finally, use transient noise to analyze noise on the entire complex-block. Due to limitations in traditional SPICE and RF tools, very few design teams perform transistor-level noise analysis at the complex-block level and many designers need to simplify even more complex sub-circuits (e.g., VCO with buffer, bias, and divider) in order to perform noise analysis. Digital fastSPICE tools do not offer noise analysis capabilities; given their level of inaccuracy, transient noise analysis would be meaningless, and digital fastSPICE tools do not have the technical foundation for periodic or oscillator noise analysis.

Table 4. Complex-Block Noise Analysis Examples

Circuit	Elements	MOS	SPICE	BDA	Speedup
PLL transient-based jitter	5.5K	5.4K	2.4 days[1]	7.8 hrs	7.4x
S-D ADC transient noise	3K	1.1K	3.1 days	6.25 hrs	10x
S-D ADC transient noise	26K	5.9K	>4.5 days[2]	24 hrs	>4.5x
2.3 GHz Dual Rx pnoise	100K	1K	DNC[3]	48 min	Infinite
VCO buf/bias/div oscnoise	8.5K	–	DNC[3]	0.5 hrs	Infinite
PLL (int-N) phase noise	5K	4K	N/A[4]	1 hr	Infinite

Notes:
1. Unacceptable traditional SPICE simulator numerical noise.
2. SPICE transient noise run not complete; the transient only time was 4.5 days.
3. Did not converge.
4. Closed-loop PLL phase noise analysis not possible with any other tool.

Berkeley Design Automation provides comprehensive, world-class noise analysis with characteristics that parallel those for its transient simulation, i.e., full accuracy, 5x-10x faster, and with 5x-10x higher effective capacity for complex blocks and complex sub-circuits within them. These capabilities make it practical for the first time to thoroughly characterize noise in sensitive complex blocks including sigma-delta ADCs, fractional-N PLLs, and SerDes/CDRs. Berkeley Design Automation also offers the industry's only non-approximate closed-loop analysis tool for integer-N PLLs – PLL Noise Analyzer™ (PNA) which utilizes the company's transient, pnoise, oscnoise/vconoise engines along with its proprietary Stochastic Nonlinear Engine™ for the full PLL. More than 10 leading semiconductor companies have verified this tool's accuracy to within 1 dB relative accuracy (2-3 dB absolute accuracy) to silicon thus proving the accuracy of the underlying engines.

Table 4 contains BDA noise analysis results on a range of production testcases. The first example is a simple jitter analysis using transient simulation only (not transient noise analysis). The traditional SPICE simulator-induced noise floor was so high that the signal was difficult to discern and the jitter numbers were unusable. The designer was able to lower the noise floor by tightening time-steps, but this resulted in unacceptably long simulations. The AFS Platform ran the circuit with acceptable accuracy, providing a sharp signal waveform and 7.4x faster than traditional SPICE (which produced unacceptable results). This PLL jitter analysis illustrates the increasing need for even more accuracy than traditional SPICE defaults.

The next two examples are transient noise analyses on sigma-delta ADCs. BDA was 10x faster in the first example. In the second example, the designer did not run transient noise analysis on traditional SPICE because transient simulation alone took more than 4.5 days. BDA completed transient noise 4.5x faster than the traditional SPICE transient only simulation on this circuit. The dual receiver and VCO with buffer, bias, and divider are examples of circuits where traditional RF simulation could not converge which made phase noise and oscillator noise respectively impossible. BDA completed each in <1 hour. The last example illustrates the company's unique PLL noise analysis technology.

RF Analysis

Many complex blocks are RF in nature and most naturally lend themselves to periodic analysis. RF designers run into accuracy, performance, and capacity limitations with traditional RF simulators (Shooting-Newton and harmonic balance) that are similar to the traditional SPICE limitations. Traditional RF simulator accuracy, performance, and memory consumption depend upon the user-selected number of sidebands or harmonics. This is not a problem for simple blocks where the tools' defaults apply, but it quickly becomes an issue for larger, nonlinear complex blocks (e.g., those with dividers). In these cases traditional RF simulator runtime and memory consumption can increase quadratically with the number of sidebands/harmonics needed – assuming the tool can even get periodic steady state (PSS) convergence. Designers are left simplifying their circuit and using a multi-pass methodology to ensure convergence, "good enough" accuracy, and reasonable runtime on computer with enough memory.

Berkeley Design Automation AFS RF uses a unique proprietary periodic analysis engine that does not tradeoff accuracy and performance. AFS RF has vastly superior PSS convergence to traditional RF simulators and delivers the equivalent of "infinite" sidebands/harmonics every run. As a result, designers can run their original circuit without simplification and utilize a 1-pass methodology that always delivers full accuracy results.

Table 5. Complex-Block Periodic Analysis Examples

Circuit	Elements	MOS	RF Sim	BDA	Speedup
Dual Conv. Rx (2 dividers)	21.5K	7.9K	DNC[1]	5.3 hrs	Infinite
Tx Modulator w/LO Gen.	16.1K	1K	DNC[1]	11.75 hrs	Infinite
Dual Rx 2.3 GHz Receiver	80K	9.5K	5 hrs	0.9 hrs	5.5x
VCO (LC Tank)	2K	0.5K	45 min	4.5 min	10x
VCO (Ring Oscillator)	8.5K	2K	DNC[1]	28 min	Infinite

Notes:
1. Did not converge (periodic steady state).

Table 5 contains a range of AFS RF comparisons with traditional RF simulators. The dual-conversion receiver and transmit modulator with LO generator did not converge in traditional RF simulation. The dual-conversion receiver contained 2 dividers. The designer in that case was able to get their traditional RF simulator to converge and complete RF analysis by removing one divider at a time. This typifies the types of simplifications, workarounds, and shortcuts that traditional RF simulation tools require. AFS RF completed the two circuits – something that no other tool had accomplished – in just 5.3 hours and <12 hours respectively.

Traditional RF simulation did converge on the 2.3 GHz receiver and the LC-tank VCO; however, AFS RF was 5.5x and 10x faster on each. This is the kind of savings that make an enormous difference on RF circuits in which designers make numerous iterations to optimize the circuit. Knowing that the results are always full accuracy is just as important. The last circuit is a relatively straightforward ring-oscillator VCO. Again, traditional RF failed to converge; AFS RF completed PSS and oscillator phase noise within 0.5 hrs.

It should be noted that AFS RF is the only simulator that produced impulse sensitivity function (ISF) information during oscillator phase noise, and it does so without any simulation overhead. Traditional RF simulators produce contribution information for every node in the circuit during oscillator phase noise. This is helpful for identifying those nodes that generate the most noise, but it can be very misleading because it says nothing about how sensitive the VCO output phase noise is to contribution from a given node. AFS RF provides contribution, sensitivity (ISF), and the product for every node in the circuit and shows how all values vary over the period. This provides VCO designers all of the analysis information they need to reliably optimize their VCOs.

5 Big Analog/RF Verification: Full-Circuit Performance Simulation

Full-circuit performance simulation is the second category of Big Analog/RF Verification. Berkeley Design Automation uses the term "full-circuit" to represent the top-level analog/RF circuitry and nominal integrated transistor-level digital logic – not a transistor-level predominantly digital design (e.g., entire SoC with SerDes). This covers a wide range of ICs such as wireless transceivers, wireline transceivers, digital TV tuners, SerDes, high-speed I/Os (e.g., PCI, SATA, etc.) power converters, data converters, and RFICs.

Most analog/RF design teams learned long ago that full-circuit performance simulation is impossible or at least completely infeasible within a reasonable timeframe. With today's top-level analog/RF circuits often surpassing 1M total elements including >250K transistors, the days when traditional SPICE could perform meaningful analysis are long past. This leaves circuit designers with the dilemma of using tools that do not have SPICE-accurate resolution – digital fastSPICE and/or mixed-mode simulation (e.g., AMS simulators) – to verify the final transistor-level implementation. This is a like trying to use a standard ruler to measure to a thousandth of an inch. At best it is possible to identify gross errors and even that might require significant judgment. Prior to BDA, the only way designers could see accurate pin-to-pin full-circuit performance was to tapeout and measure the resulting silicon.

As an example of the current limitations of full-circuit verification, consider analog/RF full circuits that include ADCs. Many design teams use digital fastSPICE or mixed-mode simulator functional verification to check their ADCs connectivity in the top-level implementation. Getting to even 1% accuracy is very difficult using either type of simulation, and without a golden reference one can never tell if they are even that close. Assuming accuracy to within 1%, it is possible to verify only the ADC's most significant 6 bits. That is hardly sufficient for today's ADCs that are routinely 12 bits or more. Although it may not be obvious, all remaining bit connections are literally unverifiable with these simulators. The only way the design team will know about any lower-order bit disconnects or misconnects is when the silicon does not meet specifications. A true SPICE accurate simulator would catch such problems with DC operating point analysis many weeks and hundreds-of-thousands of dollars sooner.

The AFS Platform enables design teams to perform the following full-circuit verification tasks that would otherwise be impossible or infeasible:

1. DC operating point analysis
2. Functional verification
3. Package & transmission-line analysis
4. Targeted performance simulation

<u>DC Operating Point Analysis</u>

Analyzing the DC operating point (i.e., a set of currents and voltages for every node that satisfy Kirchhoff's Laws for a given initial DC condition) is the simplest way to do basic circuit connectivity checks. DC operating points are also very valuable for checking basic current and voltage assumptions, determining static power consumption, and running electromigration analysis.

Even moderately complex full-circuit analog/RF designs go to tapeout without DC operating point analysis. Traditional SPICE simulators have a practical size limit of <100K total elements often fail to converge on much smaller circuits, including some as small as 10K total elements. Digital fastSPICE tools do not generate or use DC operating points. (They rely instead on designers tuning block-level simulation parameters tightly enough to ensure each block is well behaved during transient analysis.) Without the ability to perform basic connectivity checks, design teams privately report a substantial number of respins due to disconnects, including inadvertently leaving out an entire sub-circuit in one extreme case.

Table 6. Full-Circuit DC Operating Point Analysis Examples

Circuit	Elements	MOS	SPICE	BDA	Speedup
802.11 Transceiver	>150K	>100K	DNC[1]	<6 hrs	Infinite
802.11 Transceiver	>250K	>200K	DNC[1]	<2 hrs	Infinite
Dual PLL w/ Debug Logic	387K	53K	DNC[1]	1.5 hrs	Infinite
WCDM Transceiver	255K	61.7K	DNC[1]	<24 hrs	Infinite
Mobile TV Receiver	92K	61.1K	DNC[1]	3 hrs	Infinite

Notes:
1. Did not converge.

The AFS Platform consistently generates DC operating points for circuits with >1M total elements including >250K transistors. It has converged on several circuits with >2M total elements and >1M transistors. This capability alone can more than justify a tool purchase based on reducing related respins. Table 6 shows a number of circuits in which traditional SPICE could not convergence and AFS converged successfully. In each case the design team validated the resulting operating point. As noted, traditional SPICE also failed to converge on number of other large number of full-circuit and even complex-block examples throughout this paper.

Functional Verification

Design teams use digital fastSPICE or mixed-mode simulation for full-circuit functional verification in order to check connectivity and overall behavior under a variety of conditions including different configurations, different operating modes, during power-up and during reset. As pointed out above, neither digital fastSPICE nor mixed-mode simulation has adequate accuracy to check connectivity thoroughly (e.g., they cannot check low-order bit connectivity in datapaths).

Simulation accuracy is important even when verifying only functional behavior. Since small inaccuracies can lead to a qualitatively different result, it is critical that design teams be aware of the risks of false positives and false negatives. Getting “good enough” simulation with digital fastSPICE entails a process of tuning the simulator to each circuit block until the simulator produces the expected behavior. The process is to some extent self-referential (and therefore not an independent verification) in that in order to check expected behavior, the designer must tune the simulator to try to get it to produce the behavior the user expects. Using a mixed-mode simulator for functional verification has a similar limitation with respect to having to tune the circuit's behavioral models to ensure they are accurate enough.

The AFS Platform is always true SPICE accurate, so every simulation is a full performance simulation – not a functional-only simulation. The examples in Table 7 are labeled functional verification because the design team was already running or trying to run functional verification rather than a full performance simulation. In each case the design team tried to run traditional SPICE first because doing so would eliminate block-level simulator tuning and ensure the functional behavior was correct. In the first three examples traditional SPICE would not converge. In the last example, it converged but it was so slow that the design team changed approaches.

The first example was a 65nm SRAM embedded in a microprocessor. The designer had already tuned a digital fastSPICE simulator and obtained a 3.3 hr runtime, but he was concerned about very subtle behavior during reset which is impossible to check with the limited digital fastSPICE accuracy. His first run with AFS was 1.2 hours – 2.5x faster without any simulator tuning. More importantly, the AFS results were true SPICE accurate enabling the designer to accurately measure subtle behavior during reset. The full circuit in this case was more than 1M total elements.

Table 7. Full-Circuit Functional Verification Examples

Circuit	Elements	MOS	Functional	BDA	Speedup
SRAM	>1.1M	–	3.3 hrs[1]	1.2 hrs	2.5x
PCI Receiver	55.1K	54.7K	14 hrs[1]	24 hrs	0.6x
5 PPLs w/Regulator	431K	395K	N/A[2]	14 days	Infinite
I2C w/Bandgap, VCO, CP	52K	18.2K	4 days[3]	4 days	1x

Notes:
1. Digital fastSPICE runtime after extensive block-level simulator tuning.
2. Designers could not get digital fastSPICE to produce reasonable results.
3. SPICE-HDL co-simulation runtime.

In the PCI receiver example, digital fastSPICE was 14 hours versus 24 hours for AFS. AFS was within 2x without requiring any block-level simulator tuning and delivering true SPICE accurate results. Without the AFS run, the design team could never be sure if their digital fastSPICE run was producing “good enough” results or a false positive. The next example is 5 PLLs with a regulator. In this case the designer could only get digital fastSPICE to produce what the designer reported as “bizarre.” AFS converged and completed the transient run for the nearly 400K transistor circuit in 14 days. The results were accurate to the SPICE noise floor.

The next example in Table 7 is an I2C circuit that included a bandgap, VCO, and charge pump. At only 52K total elements, it was small enough for traditional SPICE to converge, but the designers aborted the transient run after a few days because they estimated it would take 40 days to complete. This type of projected runtime is far more common than some may think or wish to admit. When design teams hit this type of problem, they generally change approaches or decide the verification task is infeasible. In this case the design team adopted a traditional SPICE-HDL co-simulation approach. While doing so sacrificed some accuracy at the analog-digital interface, it got the runtime down to a reasonable 4 days. AFS ran the full-transistor level version of the circuit in the same 4 days while providing the design team the accuracy they originally required.

In addition to full-circuit functional verification, design teams may also run full-chip functional verification that includes all of the digital logic and analog/RF circuitry. Generally they choose digital fastSPICE, mixed-mode, or traditional SPICE-HDL co-simulation. There are advantages and disadvantages to each approach. Traditional SPICE-HDL co-simulation is perhaps the most natural choice because it leaves the circuitry at the transistor level and the logic at the HDL level. Unfortunately traditional SPICE simulator performance and capacity limitations have made it impractical in many cases.

The AFS Platform includes AFS Co-Simulation that supports HDL co-simulation with leading Verilog simulators and gives design teams a combination of true SPICE accuracy, 5x-20x higher performance, and 5x-10x higher capacity – all using an industry-standard SPICE-Verilog use model.

<u>Package and Transmission-Line Analysis</u>

After spending months working on detailed circuit-level verification, one of the most frustrating experiences a design team can face is silicon that does not deliver to specification due to package or transmission-line effects. Unable to adequately analyze these effects, designers must either consciously over-design or live with increasingly significant risks. Traditional SPICE runtime and capacity limitations make it impractical for this application in many cases, and digital fastSPICE simulators cannot produce the required accuracy and does not have adequate inductor and transmission-line support.

This paper categorizes this analysis as full-circuit because it is often desirable to run it at that point in the design flow. However, it is also possible to isolate the analysis to just those complex blocks that interface with the package inductors or transmission lines, as is the case examples 2-4 in Table 8.

The first example illustrates the wall that many design teams will hit soon, if they have not done so already. It is a memory in package. The memory is 244K elements, almost all of which are transistors. The package model contains 42 inductors and 145 mutual inductors. The company producing this memory IC unexpectedly encountered a significant yield loss when they moved from 90nm to 65nm. A designer traced the problem to package inductance. They had historically relied on digital fastSPICE for this analysis because their traditional SPICE simulator could not converge on such a large circuit. However, digital fastSPICE results badly mislead them at 65nm. They were able to run AFS and get true SPICE accuracy with just a 24-hour run.

Table 8. Full-Circuit Package and Transmission-Line Examples

Circuit	Elements	MOS	SPICE	BDA	Speedup
Memory in Package[1]	244K	218K	DNC[2]	24 hrs	Infinite
3GHz SerDes[3]	20K	19.4K	13 hrs	2 hrs	6.5x
Distributed VCO[4]	2K	110	30 min	3 min	10x
Video Equalizer[5]	12.7K	2.2K	36 hrs	7.3 hrs	5x

Notes:

1. Includes 42 package inductors and 145 package mutual inductors.
2. Did not converge.
3. Includes 3 package inductors.
4. Includes 2 inductors and transmission line (nport & s-parameter).
5. Includes 1800 inductors, 5 package inductors, and transmission line (nport & s-parameter).

AFS ran the 3GHz SerDes example 6.5x faster, and in the third example AFS ran the distributed VCO 10x faster. The video coax cable equalizer example includes 1800 total inductors, 5 package inductors, and a transmission line. Digital fastSPICE was not even an option. AFS completed this analysis 5x faster than traditional SPICE.

<u>Full-Circuit Targeted Performance Simulation</u>

Full-circuit performance simulation represents the ultimate challenge in Big Analog/RF Verification, and it illustrates the truly revolutionary results that are possible with Berkeley Design Automation technology.

True SPICE accuracy and full-circuit capacity are prerequisites for running performance simulation. With “only” 5x-10x performance over traditional SPICE, it is not practical to run extensive system-level behavior (e.g., realistic communications traffic through a transceiver). However, it is possible for the first time to create and run targeted performance simulations to verify known circuit worry cases such as key specifications (power, frequencies, noise, SNR) under extreme conditions. This ability gives design teams a powerful window into their silicon performance weeks and hundreds-of-thousands of dollars sooner than would be possible otherwise. Table 9 contains five full-circuit targeted performance simulations using AFS.

Table 9. Full-Circuit Targeted Performance Simulation Examples

Circuit	Elements	MOS	SPICE	BDA	Speedup
Microcontroller Analog	30K	9.1K	DNC[1]	12 hrs	Infinite
GPS Receiver	>100K	–	DNC[1]	12 hrs	Infinite
PMA Receiver	107K	11K	19.5 days[2]	68 hrs	6.5x
DDR3 SRAM	563K	110K	4.7 days[3]	14 hrs	8x
Receiver w/CDR & Equal.	515K	110K	DNC[1]	3 hrs	Infinite

Notes:

1. Did not converge.
2. Estimate – design team stopped the run due to excessive runtime.

3. Traditional SPICE required extensive initial conditions to converge.

In the first two examples traditional SPICE could not converge, so the design teams tried digital fastSPICE only to give up due to obvious inaccuracies. In just 12 hours AFS completed transient analysis for the top-level microcontroller analog circuitry. This had proven impossible with all other simulators. In the second case, the designer ran digital fastSPICE to get full-circuit power numbers for a low-power GPS receiver. When he changed the digital fastSPICE block-level simulator tuning slightly, the simulator produced results 3 orders of magnitude greater for the same netlist. The results literally changed from milliamps to amps. Needless to say, the designer thereafter did not trust digital fastSPICE. AFS delivered results that were within 20% of the designer's hand calculation and the results varied as expected across a variety of runs.

In the last three examples the design teams decided not to even try digital fastSPICE because of its insufficient accuracy. Traditional SPICE was able to converge on the PMA receiver, but the runtime was so long that the designer stopped the run which he estimated would have required over 19 days to complete. AFS completed the run and delivered true SPICE accurate results in less than 3 days. AFS was even faster compared to traditional SPICE in the DDR3 SRAM example. Traditional SPICE required extensive initial conditions to converge on the >500K total elements and >100K transistors circuit. It completed the run in 4.7 days. AFS was able to converge without the initial conditions and complete the run in only 14 hours. The last example is a receiver with CDR and adaptive equalizer. It too was >500K total elements and >100K transistors. AFS produced results that were otherwise impossible to obtain prior to measuring actual silicon.

6 A Comparative Summary

As the results from the previous two sections illustrate, Berkeley Design Automation AFS Platform provides design teams the means to perform verification on complex blocks and full circuits that is otherwise impractical or impossible. The tools' true SPICE accuracy combined with 5x-20x performance and >10M-element capacity is transforming how analog/RF design teams verify their circuits, which in turn will enable them to create even more impressive circuits in the near future.

Table 10. Analog/RF Comparative Simulation Scorecard

Analog/RF Verification Task	**Traditional SPICE**	**Digital FastSPICE**	**BDA AFS Platform**
Full Circuit			
- Targeted performance simulation			✓✓✓
- Package & transmission-line effects	✓		✓✓✓
- Functional verification	✓	✓✓	✓✓✓
- DC operating point analysis			✓✓✓
Complex Block			
- RF Multi-Tone Periodic Analysis	✓		✓✓✓
- Noise analysis (transient, periodic, osc.)	✓		✓✓✓
- Variation analysis (corners, Monte Carlo)	✓		✓✓✓
- Post-layout simulation	✓		✓✓✓
- Pre-layout simulation	✓✓	✓✓	✓✓✓✓
Simple Block			
- RF Single-Tone Periodic Analysis	✓✓✓		✓✓✓✓
- Noise analysis	✓✓✓		✓✓✓✓
- Variation analysis (corners, Monte Carlo)	✓✓✓		✓✓✓✓
- Post-layout simulation	✓✓✓		✓✓✓✓
- Pre-layout simulation	✓✓✓		✓✓✓✓

Table 10 summarizes the comparative results for traditional SPICE, digital fastSPICE, and BDA, and in so doing makes the BDA advantages strikingly clear. The rows are the specific verification tasks for simple blocks, complex blocks, and full circuits. The same verification tasks apply to simple and complex blocks. The table provides a summary rating for each verification task by simulator type. The ratings are from 0 to 4 check marks.

Check Marks	Definition
0:	Cannot adequately perform task
✓:	Minimally able to perform task
✓✓:	Performs task acceptably under some circumstances
✓✓✓:	Generally performs task well
✓✓✓✓:	Performs task exceptionally well

Traditional SPICE generally performs all verification tasks well for simple blocks. Its limited performance and limited effective capacity severely limit its applicability for complex blocks and full circuits. For complex blocks it is adequate for some pre-layout simulation and minimally performs most other tasks. However it cannot generate full-circuit DC operating points or run full-circuit performance simulations for moderately complex top-level designs.

For all of the attention given to digital fastSPICE simulators in the analog/RF domain, they provide value only for tasks that do not need accuracy. They are not at all applicable for simple blocks because traditional SPICE is much easier to use, guaranteed accurate, fast enough (in fact faster for small blocks), and has sufficient capacity. Digital fastSPICE simulators are only really applicable to functional verification at the complex-block and full-circuit level. They rate only two checks in each case because they require block-level simulator tuning and their accuracy limitations are unacceptable in many cases.

While Berkeley Design Automation focuses on Big Analog/RF Verification, its tools provide superior performance often with higher accuracy even on circuits with <1K total elements and <1-hour runtimes. Nevertheless, their real value is on complex blocks and full circuits, which is where design teams face their biggest challenges given today's highly analog/RF integrated circuits. In the former case, they provide substantially more value across the board. Yet there is room for improvement with additional accuracy, performance, and/or functionality for post-layout, variation, noise, and periodic analysis. BDA shines on full circuits being the only solution for DC operating point analysis and targeted performance simulations as well as providing vastly superior analysis of package and transmission-line effects. Again there is room for improvement. Besides the obvious improvements in performance and capacity, additional features such as co-simulation, hierarchy, parasitic reduction, and multi-core support would significantly improve its current advantages.

7 Transforming Analog/RF Design

Revolutionary electronic design automation tools do not come along often – especially those that provide substantially more accuracy, performance, and capacity without sacrificing functionality, requiring design changes, or modifying existing flows. When such tools do appear, they enable new capabilities that profoundly change the design landscape. Berkeley Design Automation Analog FastSPICE Platform is such tool.

Early adopters are able to perform Big Analog/RF Verification tasks that would otherwise be impractical or impossible. In doing so, they will undoubtedly find new, more powerful ways to apply the technology to push the envelope of state-of-the-art circuit design. In fact, over 25 companies worldwide now have this capability and are using it to gain a significant advantage in time-to-market, risk, productivity, design cost, and silicon cost at the expense of late adopters.