

Precision Circuit Analysis™ Technology:
Addressing a New Class of
Analog & RF Verification Problems

Berkeley Design Automation

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1 Executive Summary

Insatiable consumer demand, multi-GHz communications, and nanometer-scale process technologies are driving a pervasive need for high-complexity, high-frequency analog and RF circuitry. Designers have risen to the challenge with new architectures and innovative circuit techniques, yet their verification tools have fallen sorely behind. Complexity has increased many orders-of-magnitude over the last 20 years, but SPICE simulators have not kept up. RF simulators enable faster periodic analysis, but have severe limitations handling today's increasingly complex nonlinear circuits. Since neither tool can adequately verify multi-block or full-circuit designs, designers have had to improvise with mixed-level simulators, FastSPICE simulators, and test chips – each of which comes with significant penalties in terms of time, effort, and accuracy. The result is higher design costs, longer schedules, silicon respins, and over-design.

Berkeley Design Automation's Precision Circuit Analysis technology addresses the new class of analog/RF verification problems. Combining innovative applied mathematics and optimized numerical analysis, Berkeley Design Automation developed the technology from the ground up, never compromising accuracy, and proving it versus silicon every step of the way. The result is the *Analog FastSPICE™ Platform (AFS Platform)*.

The *AFS Platform* is a unified circuit verification platform that provides analog, mixed-signal, and RF (AMS/RF) design teams the ultimate in accuracy, performance, capacity, and functionality. The *AFS Platform* delivers true SPICE accuracy, 5x-20x higher performance, >10M-element capacity, and advanced analyses. AMS/RF design teams that use the *AFS Platform* from block-level design through full-circuit verification can design and verify circuits twice as fast and still perform a far more thorough verification than is possible with traditional circuit and RF simulation tools.

The *AFS Platform* is tightly integrated into the leading custom design environment, supports leading SPICE netlist formats and models, and produces standard outputs. The *AFS Platform* never trades off or compromises accuracy, performance, capacity, or functionality. Through increased productivity, 5x-20x faster turnaround times, and thorough analysis of all physical effects, design teams realize a proven 2x improvement in overall efficiency.

The *AFS Platform* enables analog and RF design teams to quickly verify problems that otherwise would be impractical or infeasible, including:

Block-Level Design

- 5x-10x faster transient
- 5x-10x faster periodic analysis
- Detailed device noise impact
- Rigorous characterization

Complex-Block Verification

- 5x-20x faster transient
- Detailed parasitic impact
- Device noise impact
- HDL co-simulation

Full-Circuit Verification

- 10M element capacity
- Targeted perf. simulations
- Inter-block validation
- Silicon-package analysis

2 Market Drivers & Technology Enablers

The demand for increasingly sophisticated, low-cost consumer electronic products is driving state-of-the-art IC technology harder than ever. The industry driver has shifted from low-volume, high-price proprietary systems in the 1980s; through mid-volume, mid-price standard systems in the 1990s; to today's high-volume, low-price consumer products. Cell phones, personal computers, PDAs, game machines, MP3 players, flat-panel displays, DVD players, home networking, wireless networking...the number, range, and variety of devices is staggering and the pace continues to accelerate. These devices require ever-increasing levels of silicon integration to meet the market's performance, price, functionality, size, and power constraints.

Semiconductor companies that service consumer markets are rapidly integrating as much analog and RF content as possible (see Figure 1.) Core business differentiation is the driver. Profitability and market capitalization multipliers increase significantly with increasing analog/RF content. Integrating analog/RF content provides premium business for the suppliers who can overcome the substantial design hurdles required to successfully deliver it. There is no shortage of demand, and that demand is driving time-to-market compression.

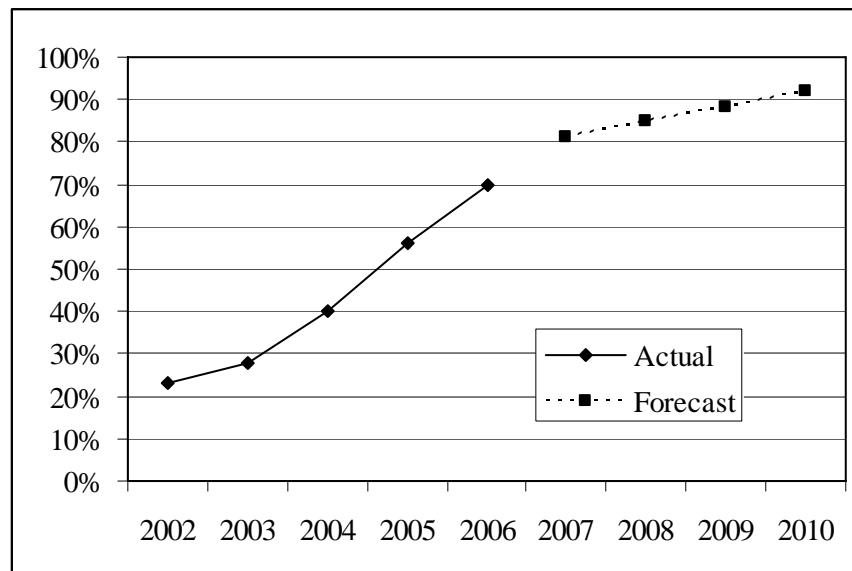


Figure 1. Worldwide ICs with >20% Analog/RF Circuitry (Source IDG)

Nearly all new electronic products require integrated wireless/wireline transceivers and high-speed I/Os. Meeting the necessary throughput, latency, and real-time interactivity demands requires increasingly complex communication standards. The number and variety of standards in particular has exploded. In wireless alone standards include WiFi (802.11a/b/g/n), WiMAX, Bluetooth, GSM, WEDGE, and W-CDMA. Each new standard advances the state-of-the-art in terms of bandwidth, power, or both. Moreover, many electronic products now require multiple standards, which are forcing design teams to look at new architectures that limit total silicon cost, size, and power consumption while meeting increasingly rigorous specifications. Processors, memory, multimedia engines,

and application-specific ICs must communicate at ever increasing speeds to keep pace with the core performance improvements in the silicon itself. Standards such as XAUI, PCI-Express, S-ATA, DDR2, DDR3, and HyperTransport are pushing silicon I/O to the multi-Gbps range.

Breakthroughs in process technologies and design approaches enable meeting these requirements. “Moore’s Law” continues to drive new process technology nodes that enable circuit complexity to double every 18 to 24 months. Advanced analog and RF designs that until recently were at .35 micron now routinely appear in 130 nm silicon. Meanwhile mixed-signal devices with complex analog functions and banks of multi-Gbps I/O are now appearing at 65 nm. Low-voltage/low-power processes are commonplace and, in fact, mandatory for many applications. At the same time, RFCMOS is becoming the standard for low-cost, high-volume wireless and wireline transceivers.

Although digital logic scales nearly linearly with decreasing process geometries, analog and RF scaling is not nearly as straightforward or forgiving, especially when it comes to nanometer-scale CMOS processes. Analog and RF designers must employ new architectures and circuit design techniques in order to take full advantage of this silicon. There is a veritable explosion in advanced techniques such as configurability, auto-calibration, direct conversion receivers, noise isolation, on-chip loop filters, multi-GHz oscillators, multi-GHz frequency dividers, integrated crystal oscillators, switched-capacitor circuits, and differential signaling. The list goes on and on. Each new approach introduces new design issues and risks along with the expected benefits.

3 A New Class of Verification Problems

The new generation of electronics products, process technologies, and communication standards (wireless, wireline, and high-speed I/O) are all hitting IC design teams simultaneously. Designers have become very innovative in terms of architecture and circuit techniques, but their circuit-level verification tools have not kept pace. More specifically, analog/RF simulators have become the bottleneck for both circuit analysis (i.e., measuring circuit characteristics for optimization) and circuit verification (i.e., ensuring circuits meets all specifications under all conditions). As a result, designers must use overly conservative design approaches, perform less optimization, lengthen schedules for verification, and take calculated risks.

The loss is significant. IC development schedules include extra weeks and months for verifying difficult potential problems such as large-circuit DC convergence, highly nonlinear PSS convergence, week-long transient runs, VCO and PLL phase noise analysis, multi-block interconnect validation, post-layout verification, and corner analysis. The number of silicon test chips and respins directly related to such issues is a more poignant and highly visible measure – especially when mask costs for nanometer-scale devices are more than \$1M each. Less obvious but just as real is the loss in potential performance, power, area, and integration designers are leaving on the table because they do not have adequate tools to analyze their circuits with silicon accuracy.

The reason is clear: today's analog/RF circuits bear little resemblance to circuits just a decade ago, yet simulator technology is largely unchanged. Consider the following list of 10 top challenges for analog and RF circuit simulators:

10 Top Challenges for Analog/RF Circuit Simulators

1. **Complexity:** Circuits have grown from hundreds of devices to over well 100K devices. Designs are now hierarchical and multi-block. They include circuits from many different designers and even different design sources (e.g., IP). *Simulators need to have the performance and capacity to handle full-circuit simulations.*
2. **Process:** Analog and RF circuits have moved from specialized micron-scale processes (e.g., bipolar) to CMOS nanometer-scale processes. This introduces new first-order factors such as flicker noise. *Simulators must accurately characterize new effects through capabilities such as nonlinear time-varying analysis for noise.*
3. **Frequency:** Circuit frequencies have moved from the MHz to multiple-GHz range for common devices. Periodic analysis is a requirement for many high-speed analog applications. *Simulators need to seamlessly handle transient and periodic analysis with silicon accuracy.*
4. **Multi-rate:** Circuits have moved to predominantly multi-frequency operation with frequencies that are orders-of-magnitude apart. Examples include ICs with integrated VCOs, high-ratio dividers, and mixers. *Simulators must perform efficient transient analysis for circuits with multiple greatly dissimilar frequencies.*

5. **Nonlinearities:** With increased integration (e.g., on-chip inductors), increased frequency operation, and new design techniques (e.g., switching architectures for low power), circuits have become highly nonlinear. *Simulators must provide robust PSS convergence in the face of increasing nonlinearities.*
6. **Power:** Low-power requirements continue driving down voltages directly affecting receiver sensitivity and making all circuitry more susceptible to noise. *Simulators must utilize the latest device models without approximation in order to deliver accurate results.*
7. **Noise:** Noise due to inherent device sources (e.g., thermal and flicker) as well as other circuitry (digital, analog, and RF) has become a first-order effect. VCOs and PLLs are particularly sensitive. *Simulators must provide silicon-accurate intrinsic and extrinsic analysis for random and deterministic noise.*
8. **Variability:** At nanometer-scales inter- and intra-die process variations greatly affect circuit characteristics and yield. Auto-calibration helps, but at the cost of additional complexity and area. *Simulators need true SPICE accuracy and high performance for extensive PVT and Monte Carlo analysis on reasonable-sized circuits.*
9. **High-Q:** High-Q circuits are increasingly combined with a highly nonlinear block like a hard-limiter. The resulting circuits are extremely difficult to achieve convergence and simulate. *Simulators must include specific algorithms for accurate, fast analysis of high-Q circuits.*
10. **Parasitics:** Wiring dramatically affects performance at GHz frequencies, especially in nanometer-scale CMOS processes. Parasitics are required to verify sensitive blocks and their interconnections. *Simulators need the true SPICE performance and capacity to handle post-layout parasitic verification for multi-block circuits.*

4 Limits of Traditional Circuit Simulators

Circuit designers face very difficult choices in applying traditional simulators to leading-edge verification problems. At the most basic level design teams must continuously ask themselves how to accurately verify their design as quickly as possible. The answer is becoming more difficult with more complex designs. Designers would like to be able to run true accuracy simulations on large designs with reasonable runtimes and without any special modeling or tuning. For transient, true accuracy simulation requires a traditional SPICE simulator, but SPICE runtimes have become increasingly impractical for GHz circuits implemented in nanometer-scale silicon.

Design teams generally structure their tasks around expected simulation runtimes, e.g.:

- **Daytime:** nominally up to 2 hours: analyze and verify blocks
- **Overnight:** nominally 12 hours: verify complex blocks (e.g., VCO) and simple multi-block circuits
- **Weekend:** nominally 60 hours: verify multi-block circuits, post-layout blocks and simple corners (PVT), special cases (e.g., PLL locking)
- **Extended:** nominally up to 1 week: verify complex multi-blocks (e.g., full transceiver), post-layout multi-blocks (e.g., PLL), extensive corners (PVT/Monte Carlo), critical cases (e.g., long PLL locking)

Designers simply cannot allow daytime tasks to require an overnight run, overnight tasks to require a weekend run, weekend tasks to require extended runs, or extended runs that become infeasible. Instead, they find other methods that let them get their job done, albeit at the expense of accuracy and productivity.

SPICE Simulator Limitations

The most obvious method to address the true accuracy simulation runtime problem is to partition circuits into smaller blocks, e.g., adding a level of hierarchy. While this can get block-level runtimes to acceptable levels at full accuracy, the result is significant lost productivity in partitioning, testbench creation, simulation, and analysis for many additional blocks. This approach does not address the multi-block runtime problem. In fact, it makes it worse because the design team likely needs to perform an additional level of multi-block simulation due to the additional hierarchy. Moreover, designers do most of their optimization at the block level, in part because they require fast simulation iterations in order to tweak their circuits. Creating smaller blocks makes it much more difficult to optimize the overall circuit and, therefore, less likely that designers will do so.

Transient runtimes are not the only problems for today's SPICE simulators. Design teams need to perform DC analysis to check for correct power behavior, excess leakage currents, excess power dissipation, etc. DC convergence has become a difficult-to-impossible task for many complex circuits. Designers are used to using increasingly elaborate and time-consuming procedures to get DC operating points, including making

minor circuit changes (e.g., eliminating small floating resistors and simplifying models), providing extensive node estimates, changing simulation parameters (e.g., iteration limit and step size), loosening tolerances, ramping voltages using transient, and partitioning the design. These approaches are time consuming and can help only so much. Unable to perform DC analysis in simulation, design teams increasingly have to risk going to silicon anyway.

Mixed-level Simulator Limitations

Many design teams have taken to using mixed-level simulation (e.g., AMS) to augment circuit-level simulation. This offers many benefits, including efficient early system-level analysis and a flexible, realistic testbench environment for block and multi-block circuit simulation. While this approach obviously does nothing to address the block-level SPICE runtime issues, it holds the promise of addressing multi-block runtimes if the block-level behavioral models are accurate enough. However, creating and maintaining accurate models can be tricky, time consuming, and error prone. The required and actual levels of accuracy are very difficult to determine, and the act of increasing model accuracy itself requires ever increasing time and effort. For these reasons, circuit designers generally trust models for only system-level analysis and functional testing. They know that the only way to guarantee SPICE accuracy is to simulate the circuit itself.

FastSPICE Simulator Limitations

A third alternative, FastSPICE simulation, sacrifices both circuit and simulator accuracy in order to increase performance. FastSPICE often provides orders-of-magnitude speedup versus SPICE in digital applications, and its accuracy is good enough for such applications. However, FastSPICE simulators get this speedup by using simplifying assumptions and approximations that sacrifice accuracy that is essential to analog and RF applications. These simplifications include partitioning, using alternative device models (e.g., table lookup or piecewise linear models), evaluating based on events, device and circuit approximations (e.g., grounding floating capacitors and inductor approximations), and eliminating time-step convergence and truncation error checking. These simplifications can result in grossly incorrect behavior if not properly managed.

Applying FastSPICE to analog and RF designs requires tuning the simulator accuracy to each individual block in order to get the highest performance, while maintaining reasonable circuit behavior. Of course there is always a risk that apparently accurate-enough block behavior leads to completely inaccurate full-circuit behavior, especially for designs that have complex feedback paths. Nevertheless, many design teams use FastSPICE for long simulations in which accuracy is not paramount, e.g., functional multi-block connectivity. In such applications, designers often spend multiple weeks in block-level FastSPICE tuning. Successful tuning requires good understanding of the entire circuit. Empirically, the result is typically 3x-5x faster simulation than SPICE for applications that are not accuracy sensitive. Despite the high setup costs and low accuracy, FastSPICE simulation has enabled designers to verify functional behavior that would not otherwise be visible until silicon.

FastSPICE simulators' inherent inaccuracy fundamentally limits its applications in analog and RF designs. FastSPICE simulations can perform only basic functional verification. Its results are not accurate enough for performance analysis (e.g., meaningful node or specification measurements). Consider the simulation of an A/D converter. Tuning a FastSPICE simulator to within 1% of SPICE while maintaining a reasonable performance advantage is difficult. At that accuracy, the simulator can verify only the first 6 significant bits of connectivity – bits 7 and beyond are masked by the simulator inaccuracy. FastSPICE simulators have proven unable to provide the accuracy needed for performance simulations (e.g., simulations in which specification or node measurements are critical). Moreover, tuning a FastSPICE simulator to near-SPICE accuracy generally results in slower performance than SPICE.

RF Simulator Limitations

Many design teams begin using RF simulators specifically in order to perform VCO phase noise analysis. Again, the simulators have not kept up with the problem. RF simulators use linear approximations to calculate noise. However, accurate phase noise characterization for VCOs and PLLs requires a nonlinear analysis that current RF simulators do not provide. This produces non-physical results like infinite total power in an oscillator. For PLLs, the standard approach is to use RF simulation to get block-level estimates, and then create top-level behavioral models to calculate the overall noise. This approach produced acceptably accurate results for MHz circuits at 0.25 μ . However today's multi-GHz wireless, wireline, and high-speed I/O standards have critically tight phase noise and jitter specifications. The current approach has proven to be grossly inaccurate at low-offset and high-offset frequencies for nanometer-scale GHz circuits needed to meet these specifications.

Convergence problems are not unique to DC analysis. PSS convergence is an even bigger problem for high-frequency analog and RF designs. Today's RF simulators are notoriously poor at PSS convergence. Again, the increasingly elaborate procedures only take designers so far. At the limit designers must further partition their design wherever possible, thereby incurring extra time, effort, and risk missing problems between blocks. Where not possible or cost effective, circuit designers again end up using increasingly expensive silicon to verify their circuit.

Multi-rate circuits are another difficult problem for today's simulators. The issue is how to efficiently simulate circuits with frequencies that are either greatly disparate (carrier and modulation) or closely matched (producing a low beat frequency). SPICE simulators require time-step rates based on the highest frequency signal, yet need to run long enough for the lowest frequency signal. This often results in infeasible multi-week transient runs. Harmonic balance analysis is an attractive alternative for mildly nonlinear circuits. However, harmonic balance rapidly becomes impractical with increasing circuit nonlinearity and size; the simulator grinds to a crawl or runs out of memory when it needs to include hundreds of harmonics in order to achieve convergence or maintain accuracy. Quasi-periodic steady state (QPSS) analysis has been another practical alternative in some cases. However, as implemented in current simulators, it suffers from many of the same limitations cited above for PSS analysis. It is often feasible to apply

only one large signal and one or two moderate signals (currently limited to 3 harmonics), which is not sufficient to fully characterize many specifications of interest (e.g., blocker analysis and receiver sensitivity).

Simulator Limitations Summary

There are many additional problems from post-layout verification to extensive corner and configuration verification. Yet, the pattern above is clear. Simulation capabilities (performance, convergence, and analysis) have not kept up with the increasingly demanding verification needs. Using time, effort, and considerable ingenuity, designers have pushed the technology far past what the simulators' original developers ever contemplated. Design teams have come up with alternative approaches using mixed-level simulation, FastSPICE simulation, and even test chips to push the limits even further. However, they have hit the breaking point for a large and growing number of applications. Design teams increasingly face taking circuits with known high risks directly to silicon. In doing so they face the nightmare scenario of silicon that misses a critical specification not by some gross amount that they have a chance of diagnosing, but by 1dB or 1ps – problems that require true accuracy, full-circuit verification before tapeout.

5 Precision Circuit Analysis Technology

Berkeley Design Automation was founded specifically to fill the growing gap between traditional circuit simulation and silicon for leading-edge analog and RF designs. The company's Precision Circuit Analysis technology is the first fundamental breakthrough in analog/RF verification in more than a decade. Combining innovative applied mathematics with advanced numerical optimization techniques, Berkeley Design Automation developed the technology from the bottom-up – never compromising accuracy. The result is true SPICE accuracy transient and periodic analysis that is 5x-20x faster than SPICE, with no block-level tuning (see Figure 2). Circuit design teams have validated Precision Circuit Analysis technology versus silicon on over 100 production designs from 0.5 μ down to 65nm.

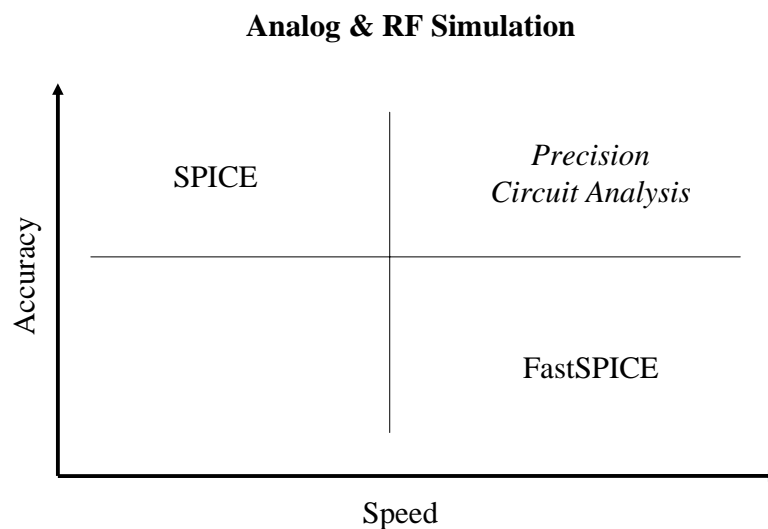


Figure 2. True SPICE Accuracy, 5x-20x Faster, No Tuning

Precision Circuit Analysis technology is based on a proprietary combination of innovative applied mathematics and optimized numerical analysis. Traditional SPICE and RF simulators have mathematical foundations that go back over 30 years. Their mathematics was practical, if not optimal, for those circuits. Today's circuits have radically different characteristics. Recognizing this, Berkeley Design Automation identified mathematics proven in non-electronic domains that have similar characteristics to today's leading-edge circuits, e.g., multi-rate, nonlinear, and stochastic. Although these techniques showed great promise, it was not possible to retrofit them into an existing circuit simulator without losing their accuracy and performance advantages. Applying them required developing a new simulator from scratch.

Berkeley Design Automation turned this apparent disadvantage into an advantage. The company used the opportunity to apply optimized numerical analysis techniques to every component in the simulator. Among the new core components are a fast sparse matrix solver, globally convergent nonlinear solvers, efficient stiff differential algebraic equation solver, unified time/frequency engine, and stochastic nonlinear engine. The

development team followed one simple rule – never compromise accuracy, then get as much performance as possible. Unlike digital FastSPICE simulators, Precision Circuit Analysis technology makes no simplifying assumptions or approximations. It solves the original device equations on the original circuit with accuracy that is equivalent to or exceeds SPICE simulators. This means that it needs no block-level tuning and always provides true accuracy at every node in the circuit; hence every simulation is a full performance simulation. The result is breakthrough technology that can address a whole new class of verification problems.

6 Technology Example: Industry's First Multi-Rate Transient Engine

The Precision Circuit Analysis multi-rate transient engine exemplifies the technology's superiority when applied to advanced analog/RF designs. Transient accuracy and performance are the most important characteristics in any circuit simulator. Achieving outstanding results requires core technology that is well matched with the target circuit characteristics.

SPICE circuit simulators have single-rate transient engines, i.e., transient engines that are based on single-rate mathematics. This means their differential algebraic equation (DAE) solvers are efficient at evaluating only nonstiff DAEs. Hence SPICE simulators are efficient for circuits in which there is a single frequency or tight frequency range. Traditional single-rate transient engines become increasingly inefficient as the number and disparity of frequencies within a circuit increases. Of course this is exactly what has happened in circuits over the past decade. Today's complex circuits commonly have multiple frequencies that range several orders-of-magnitude. While SPICE simulators continue to provide high accuracy for these circuits, their performance has become untenable. See the left diagram in Figure 3.

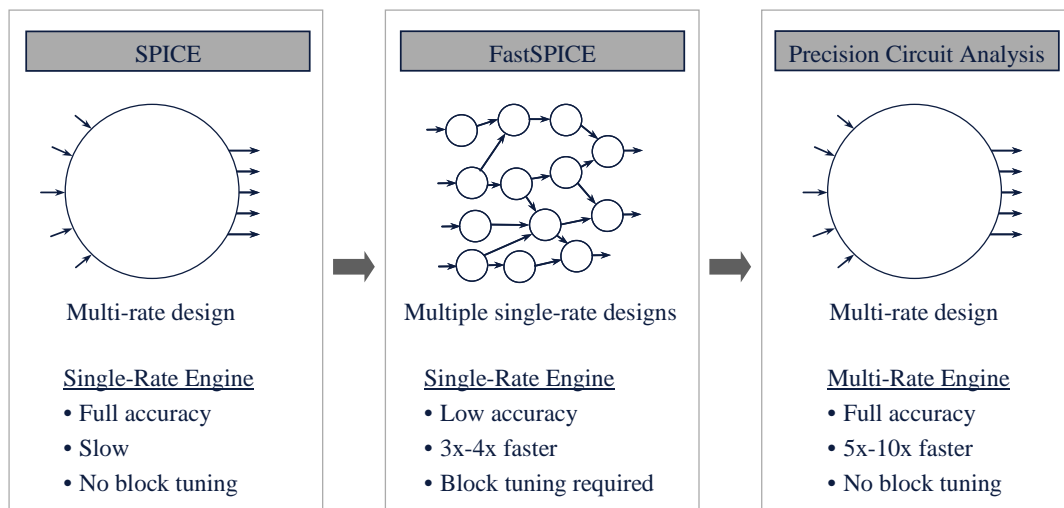


Figure 3. Multi-Rate Design and Transient Engine Comparison

One way to get higher performance is to partition a design into many smaller, simpler circuits (e.g., single-rate or simple multi-rate circuits); tune the simulator settings for each block; and then simulate the blocks together in an event-driven manner. This is exactly the approach that FastSPICE simulators use. At their core, FastSPICE simulators contain a single-rate transient engine that is efficient at evaluating only nonstiff DAEs. They contain features to partition designs into blocks that run semi-autonomously. Users must understand the simulation requirements for each block in order to tune them with the goal of maximizing performance while maintaining sufficient accuracy for functionally correct overall behavior. In addition to being extremely time consuming – often requiring weeks for sufficient block-level tuning – this approach is inherently problematic for tightly coupled circuitry. FastSPICE simulators include a number of other features, such

as device model simplification, which enhance speed at the expense of accuracy. See the middle diagram in Figure 3.

Berkeley Design Automation has developed the industry's first multi-rate SPICE transient engine. Rather than break the design up into multiple single-rate designs, the multi-rate transient engine treats the circuit as a whole just as SPICE simulators do. Hence, it requires no block-level tuning. However, the mathematical foundations for the Precision Circuit Analysis multi-rate transient engine are very different from those of SPICE. The multi-rate engine's underlying mathematics is highly efficient at solving the stiff DAEs. It makes no approximations. The multi-rate engine solves the same device equations as SPICE. It just does so in a fraction of the time. The result is true SPICE accuracy with an increasing performance advantage as the circuit size, number of frequencies, and frequency disparity increases – all three of which tend to be correlated. The multi-rate transient engine provides SPICE-equivalent or better performance for even small single-rate circuits and has capacity that is similar to traditional SPICE simulators. See the right diagram in Figure 3.

7 Precision Circuit Analysis Tools

The *Analog FastSPICE™ Platform (AFS Platform)* implements the Precision Circuit Analysis technology. The *AFS Platform* is a unified circuit verification platform that provides analog, mixed-signal, and RF (AMS/RF) design teams the ultimate in accuracy, performance, capacity, and functionality. The *AFS Platform* delivers true SPICE accuracy, 5x-20x higher performance, >10M-element capacity, and advanced analyses.

The *AFS Platform* is a modular single-executable implementation that guarantees identical waveforms to traditional SPICE every run regardless of the size, complexity, or type of analysis. Its modularity enables independent optimization of every component, while ensuring all functionality works together seamlessly.

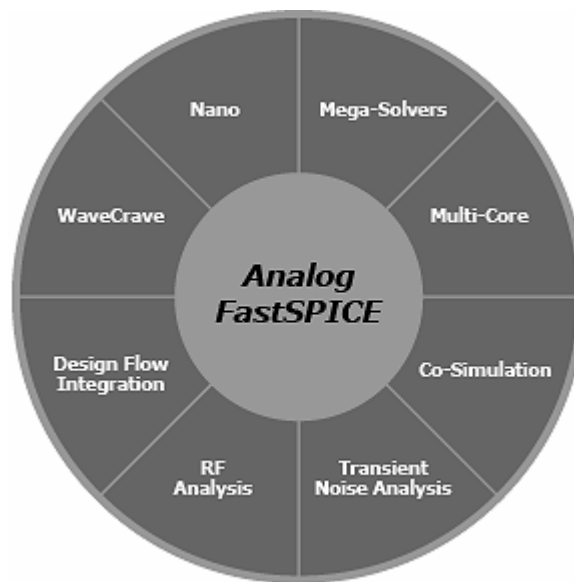


Figure 4. *AFS Platform* Functionality

At the block level, the *AFS Platform* delivers the fastest iterations, the only nanometer-accurate device noise analysis, and unparalleled corner and variation analysis. Complex blocks such as ADCs, PLLs, and SerDes require long runtimes with detailed parasitics including device noise effects—runs only possible with the *AFS Platform*. Finally, the *AFS Platform's* capacity and performance enable full-circuit DC operating point generation and performance simulation—with complex package models and co-simulation of top-level digital logic.

The *AFS Platform* includes *AFS RF Analysis (AFS RF)* targeted at device noise and RF analysis of periodic circuits. *AFS* full-spectrum periodic noise analysis (pnoise) computes the noise of periodically-driven circuits such as mixers, switched-capacitor filters, phase detectors, and charge pumps. *AFS* full-spectrum oscillator noise analysis (oscnoise/vconoise) computes the phase noise of periodic autonomous circuits such as VCOs (LC-tank and ring-oscillator circuits) and crystal oscillators.

8 Precision Circuit Analysis: Applications and Results

Berkeley Design Automation's Precision Circuit Analysis tools are uniquely able to handle complex verification problems that traditional SPICE, RF, mixed-level, and FastSPICE simulators cannot handle. The tools are particularly valuable for verification tasks that otherwise would be impractical (i.e., require excessive time, excessive effort, or compromises in accuracy) or infeasible (e.g., circuits that do not converge, multi-week transient runtimes, and silicon-accurate noise analysis). Target applications include:

- Full transceivers (802.11a/b/g, WiFi, GSM, 3G, 4G)
- High-speed I/O (SerDes, DDR2/3, PCI-Express, XAUI)
- Multiple-block (interconnect, performance, functional verification)
- Highly-nonlinear RF blocks (VCOs, PLLs, mixers, high-Q crystal oscillators)
- Post-layout circuits with 1M+ elements
- Extensive corner (PVT including Monte Carlo) & configuration verification

Precision Circuit Analysis tools have been proven on over 100 designs ranging from 100s to >100K devices and more than 10 process nodes at a number of popular and captive foundries. As shown below for each of the tools, the results are consistently and dramatically superior to traditional simulation.

Circuit	Size	Process	SPICE	BDA	Delta
802.11 #1	107,264	0.18	1:15 hrs	0:09 hrs	8.3x
802.11 #2	50,754	0.18	8:31 hrs	1:18 hrs	6.6x
802.11 #3	34,970	0.18	8:56 hrs	1:45 hrs	5.1x
802.11 #4	25,522	0.18	6.25 days	0.6 days	10x
AGC	15,000	0.13	13:15 hrs	0:22 hrs	36x
DDR2	10,000	0.13	10.7 days	1 day	10x
SerDes #2	8,600	0.09	10.3 days	1.7 days	6.1x
Consumer #1	5,500	0.18	3:10 hrs	:29 hrs	6.5x
SerDes #1	4,200	0.13	5.4 days	0.3 days	18x
Serial I/O	3,400	0.13	16.8 days	1.5 days	11x
System Clock	1,800	0.25	16.5 days	.95 days	17x
SoC Clock	1,700	0.18	12 days	.35 days	34x
Consumer #2	1,612	0.13	9.8 days	2.2 days	4.5x
Networking	1,154	0.13	6:12 hrs	1:12 hrs	5.2x
Flash	1,000	0.09	1:08 hrs	0:03 hrs	23x

Table 1. *AFS Platform* True SPICE Accuracy Transient Performance

AFS Platform Results

The *AFS Platform* true SPICE accuracy transient performance for a representative sample of circuits is shown in Table 1. The circuits range two orders-of-magnitude in complexity, from 1K devices to over 100K devices. The applications include full wireless transceivers, high-speed I/O for SoCs and memory, complex analog/mixed-signal ICs, and consumer ICs. All of these are production designs with the original testbench and

circuit setup. They are all out-of-the-box results, i.e., the user did not tune the simulator algorithms or perform block-level tuning. In each case, the original circuit designer compared critical waveforms and node-specific measurements with their current SPICE simulator results and validated that the *AFS Platform* provided true SPICE accuracy.

Table 2 shows the superior global DC convergence results for the *AFS Platform* on three designs – two 802.11 transceiver circuits and a post-layout dual PLL with debug circuitry for a 65nm processor. In all three cases, the original designer was unable to achieve convergence with their original SPICE simulator despite extensive time and effort. In each case, the *AFS Platform* converged out-of-the-box, i.e., with no simulation algorithm changes or block-level tuning. In fact, all converged on the first run. In two cases the designer had the result within 2 hours and in the third within 6 hours.

Circuit	Size	Process	SPICE	BDA	Notes
802.11 #5	255,415	0.13	DNF	1:43 hrs	
802.11 #6	168,469	0.13	DNF	6 hrs	
Dual PLL	>1,1M	0.065	DNF	1.35 hrs	Post layout

Table 2. *AFS Platform* DC Convergence

AFS RF Results

AFS RF Analysis has proven its superiority in a number of difficult verification problems versus current RF simulators. Table 3 shows the results for seven circuits that range more than two orders of magnitude in complexity and multiple applications (transceiver, networking, and consumer). In four of the circuits, the designers could not get their current RF simulator to complete PSS convergence – including on a highly nonlinear design that was just 323 devices. *AFS RF* converged on all of the designs out-of-the-box. Even in cases where the traditional RF simulator was able to converge, *AFS RF* outperformed it by 10x-60x – without compromising accuracy.

Circuit	Size	Process	RF Sim		BDA		Delta
			Converge	Runtime	Converge	Runtime	
Digital TV #2	8,590	0.18	No	N/A	Yes	28 min	---
Networking #2	6,549	0.11	No	N/A	Yes	10 min	---
Digital TV #1	6,000	0.18	No	N/A	Yes	14 min	---
Wireless #1	2,000	0.18	Yes	45 min	Yes	4.5 min	10x
Wireless #2	1,700	0.18	Yes	100 min	Yes	1.6 min	60x
Networking #1	1,233	0.13	Yes	40 min	Yes	4 min	10x
Wireless #3	323	0.18	No	N/A	Yes	10 min	---
Wireless XO	115	0.18	Yes	4 hrs	Yes	76 sec	200x

Table 3. *AFS RF* PSS Convergence and Performance

The simulation times in each of the cases in which the RF simulator converged are at the upper-end of what most designers consider acceptable runtimes for iterative design. In these cases, *AFS RF* delivered 10x faster simulator turnaround, enabling much faster

design iterations. With *AFS RF* designers can finish significantly faster and better optimize their blocks. Alternatively they can partition their design less. Doing so saves partitioning time and effort, avoids having to verify interfaces and interactions between smaller blocks, and enables superior overall circuit optimization.

PLL Noise Analysis Results

Precision Circuit Analysis includes a stochastic nonlinear engine that directly computes phase noise without approximations. The result is highly accurate phase noise that circuit designers have independently proven time-and-time again versus actual silicon across a wide range of process technologies. The results for two such PLLs are shown in Table 4 and Table 5 below. Each table shows the results for three different PLL settings. The Differences column shows the differences in absolute phase noise measurements. Model inaccuracies are the primary contributor to the absolute difference. The difference of the differences is the relative accuracy, which is a measure of how closely the simulation results track the silicon results under varying PLL conditions. This approach essentially eliminates model inaccuracies and shows a correlation of ~1 dB for a wide range of PLLs, including these circuits.

Phase Noise (dBc/Hz)	BDA	Silicon	Difference
PLL Setting 1	-97.5	-95	2.5
PLL Setting 2	-87.3	-85	2.3
PLL Setting 3	-97.2	-94	3.2

Table 4. ~1 dB Relative Accuracy for 0.18 μ Wireless Frequency Synthesizer

Phase Noise (dBc/Hz)	BDA	Silicon	Difference
PLL Setting 1	-114.8	-114	0.8
PLL Setting 2	-114.3	-114	0.3
PLL Setting 3	-108.8	-108	0.8

Table 5. ~1 dB Relative Accuracy for 0.25 μ SerDes PLL

9 Precision Circuit Analysis Transceiver Example

Consider the impact that Precision Circuit Analysis technology can have on an 802.11 transceiver design implemented in RFCMOS (see Figure 5 for an example). While a traditional RF simulator is sufficient for many simple blocks, the design contains a number of complex highly nonlinear blocks such as an LNA with mixer, a VCO with buffer and bias circuit, and a crystal oscillator. These blocks would require extensive setup to achieve PSS convergence, if at all possible. They would also require long runtimes, making optimization difficult and time consuming. *AFS RF* provides robust PSS convergence greatly reducing if not eliminating PSS convergence setup. It also delivers 5x to 10x faster performance than traditional RF simulators. The superior *AFS RF* convergence, accuracy, and performance characteristics makes it practical to perform less partitioning, more quickly optimize larger circuits, verify even complex blocks with post-layout parasitics, and perform 5x to 10x more corner analysis prior to silicon.

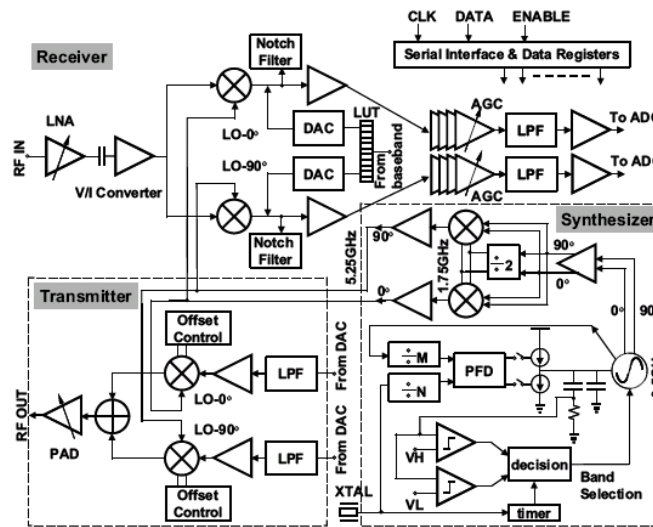


Figure 5. Direct Conversion CMOS Tx/Rx for IEEE 802.11 WLANs, ISSCC 2003

VCO noise analysis is also problematic with RF simulators, often producing self-inconsistent results that raise serious questions regarding the actual noise parameters prior to silicon. *AFS RF* produces VCO noise analysis within ~1dB relative accuracy to silicon; hence design changes that result in lower noise in simulation will also result in lower noise in silicon. The device contribution and sensitivity results together provide designers with the information they need to make intelligent tradeoffs between performance, power, area, and noise.

Once individual blocks are complete, the design team needs to perform multi-block verification. With traditional SPICE simulators, DC convergence problems often limit the size of the overall circuit that they can simulate at the transistor level. Even when convergence completes, runtimes quickly run into multiple weeks limiting the total circuit size it is practical to verify, as well as the number of configurations. The design team could use a traditional digital FastSPICE simulator, but doing so would require

multiple weeks of setup and provide only basic functional verification. The overhead prohibits verifying many different multi-block combinations. Its inaccuracy makes performance simulations impossible and post-layout verification virtually meaningless.

The *AFS Platform* changes this scenario dramatically. The tool's global convergence is reliable and robust even when applied to the entire transceiver. The 5x to 20x performance advantage makes pure transistor full transceiver simulations practical. It is feasible to run simulations that would take even a month in a SPICE simulator. Because there is no block-level tuning, it is easy to simulate many different multi-block combinations. Every *AFS Platform* simulation has true SPICE accuracy; hence every simulation is a performance simulation. The tool's accuracy and performance also makes post-layout, PVT, and configuration verification practical.

10 Conclusion

This paper has described how market drivers and technical enablers are pushing advanced analog and RF circuits to new levels of complexity, multi-GHz frequencies, and nanometer process technologies. Combined with increasingly challenging physical characteristics such as highly nonlinear multi-rate circuits with high-Q factors, the result is a new class of verification problems that traditional SPICE, RF, FastSPICE, and mixed-level simulation simply cannot handle. With considerable time, effort, and ingenuity, designers have pushed these simulators beyond all reasonable limits.

Recognizing these problems, Berkeley Design Automation developed groundbreaking Precision Circuit Analysis technology from the bottom up. Combining applied innovative mathematics and optimized numerical analysis, Precision Circuit Analysis delivers true SPICE accuracy, 5x-20x higher performance, vastly superior DC and PSS convergence, and ~1dB relative noise accuracy. Berkeley Design Automation's *Analog FastSPICE Platform*, based on the Precision Circuit Analysis Technology, is silicon-proven on over 100 designs and across a wide range of process technologies. All of the tools readily fit into existing design flows including full netlist, model, and environment compatibility.

With Precision Circuit Analysis, designers can analyze and verify circuits that would otherwise be impractical or infeasible. Full transceiver performance simulations, DC convergence of >1M element post-layout circuits, silicon-accurate multi-GHz nanometer VCO noise analysis, and extensive high-speed I/O corner analysis – Precision Circuit Analysis makes it not only possible, but imminently practical.