

Characterize Nanometer Analog/RF Circuits

As analog and radio-frequency (RF) designs move to lower process geometries, rigorous circuit characterization is becoming increasingly important. The associated computation requirements are large. And they're growing exponentially with increasing circuit complexity, nanometer physical effects, and statistical variations. Yet characterization is only going to grow more difficult because of market demands like ever-tighter specifications, short time-to-market windows, and higher levels of integration.

Analog/RF characterization is the process of ensuring that circuits meet all performance specifications over their target parameter ranges. This process also includes realistic physical effects and manufacturing variations. To date, most design teams have dealt with small process geometries by incrementally extending historical corners-based approaches and selectively supplementing corners analysis with statistical techniques. Given the costs and risks involved, it behooves design teams to move to a systematic approach that uses an up-front, quantitative, circuit-specific characterization plan. In such a plan, the schedule, design cost, circuit margin, and risk tradeoffs are explicit. This type of approach lets design management assess the adequacy of its computational environment and tooling for characterization.

CHARACTERIZATION WITH NANOMETER PHYSICAL EFFECTS

Analog and RF circuits are increasingly subject to first-order physical effects that can fundamentally limit circuit performance. Such effects include device noise, detailed parasitics, and device mismatch. These exploding requirements are shown in Figure 1.

Device noise affects a wide range of circuits including phase-locked loops (PLLs), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), SerDes, clock and data recovery (CDRs), receive chains, and transmit chains. In nanometer process nodes, these circuits require full-spectrum device noise analysis. This analysis provides results that are proven to match within 1 to 2 dB of actual silicon. Parasitics can profoundly affect circuit performance

including device noise. Accurate characterization requires robust, fast circuit simulation with detailed parasitics rather than estimates or uncalibrated reduction.

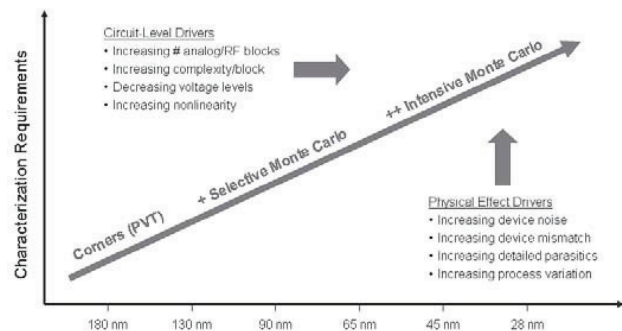


Figure 1: This chart provides a snapshot of today's exploding characterization requirements.

Device mismatch is critical for circuits that use matched devices, such as current mirrors, voltage dividers, bandgap references, and feedback networks. Mismatch effects can rapidly degrade circuit performance. Simply increasing area no longer necessarily improves mismatch. Moreover, many nanometer circuits are simply too size and power sensitive to use sizing except where absolutely necessary. Instead, Monte Carlo simulation is now a requirement for analyzing device mismatch.

QUANTITATIVE STATISTICAL APPROACHES

Design teams have historically relied upon corners-based approaches to ensure that circuits meet the specification at extreme conditions. Although corners will continue to be important—especially at higher levels in the hierarchy—corners analysis is no longer sufficient. Corners are often too pessimistic for die-to-die process variations and cannot model intra-die local variations. Instead, design teams must increasingly use statistical approaches, such as Monte Carlo simulation, to quantify the performance impact of die-to-die process variations and intra-die device variations.

Typically, designers use Monte Carlo to get a general “feel” for their circuits and identify obvious issues. Most designers don't fully leverage the quantitative statistical results. Properly applied, Monte Carlo results can quantify

the relationship between circuit measurements, iterations (for example, sample size), and risk (confidence levels). This can provide the basis for characterization planning that incorporates those tradeoffs up front (before any simulation). These quantifiable design tradeoffs are shown in Figure 2.

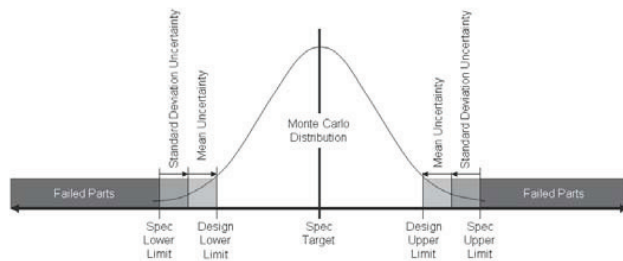


Figure 2: Quantifiable design tradeoffs can be attained using statistical approaches.

The statistical foundations for systematic characterization planning are estimated mean and standard deviation confidence intervals. Simply put, these intervals define the ranges within which the mean and standard deviation will fall for a given confidence level. Designers can trade off increasing the number of Monte Carlo iterations against the predicted statistical uncertainty. This choice enables them to determine the circuit targets needed to meet the specification.

TOOL AND ENVIRONMENT REQUIREMENTS

Analog/RF characterization is computationally intensive. With literally hundreds of iterations to run on complex blocks like PLLs, ADCs, DACs, receive chains, and high-speed I/Os, it's no longer practical to fully characterize circuits with traditional SPICE tools on single-core machines.

In a recent Berkeley Design Automation survey of designers at 10 semiconductor companies worldwide, the majority of designers working on nanometer analog/RF circuits responded that they include or try to include device noise, detailed parasitics, and device mismatch (via Monte Carlo simulation) for their circuits. Every designer stated that he or she is limited in terms of simulation runtime and licenses. Some have moved to distributed environments. But these designers reported related issues, such as contention with other jobs, use model complexity, and network issues.

A new generation of nanometer circuit-verification tool is emerging that provides the accuracy, performance, capacity, and functionality required for intense analog/RF

characterization needs. For example, the Berkeley Design Automation Analog FastSPICE Platform (AFS Platform) provides the following: nanometer SPICE accuracy; 5X to 10X higher performance than traditional SPICE on a single-core, 10-million-element capacity; and a full complement of analog, device-noise, and RF analyses.

This platform integrates into existing single-machine and distributed characterization environments. For characterization applications, however, the AFS Platform includes a multicore parallel operating mode (MCP) that automatically distributes corner, sweep, and Monte Carlo iterations to separate cores on multicore machines. Being 5X to 10X faster on a single-core, AFS MCP provides 25X to 50X higher throughput than traditional SPICE on a single machine. Designers can replace 25 to 50 traditional SPICE simulator licenses running on multiple computers with one eight-core machine that uses just three AFS licenses. Figure 3 shows sample results of AFS MCP.

Circuits				Speedup versus 1-core AFS		
Circuit	Analysis	Elements	MOS	2 Core	4 Core	8 Core
VCO	transient	1.5K	1.2K	2.0x	3.3x	5.0x
ADC	transient	17K	15.4K	1.9x	3.6x	5.7x
DLL	transient	127K	4.3K	N/A	3.9x	7.8x
Transmitter	transient	750K	15.2K	1.9x	3.7x	7.0x
Mixer	RF	26	3	1.9x	2.8x	4.5x
Ring VCO	RF	101	80	1.9x	3.8x	5.2x
LNA IP3	RF	174	8	1.7x	2.2x	4.0x
DSM IP3	RF	1.4K	135	1.8x	3.5x	4.5x

Figure 3: Shown are AFS multicore parallel results.

Characterizing analog/RF circuits is a computational bottleneck that's only getting worse with growing circuit complexity and nonlinearity. Nanometer processes introduce new physical effects that fundamentally limit circuit performance—most notably device noise, detailed parasitics, and device mismatch. Process and device variations require adopting statistical approaches. By using basic statistical principles, design teams can create characterization plans that explicitly trade off simulation runtime, circuit margin, and risk. With new-generation nanometer circuit-verification tools, design teams can efficiently and effectively characterize their nanometer analog/RF circuits. ♦

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